

The diagram illustrates the system architecture of the Intel Atom Z670. The central components are the CPU (Arrandale 2 Core, Page 3~8) and the PCH (Page 13~21). The CPU is connected to the PCH via FDI and DMI interfaces. The PCH is connected to the KBC (ENE 3926, Page 23) via LPC BUS and EC-SPI. The KBC is connected to various peripherals including Keyboard, Touch Pad, LID, Smart Fan, LED, and SPI BIOS. The PCH is also connected to various storage devices (HDD, ODD) via SATA, and to various USB devices (USB0, USB1, USB2, USB3, USB4, USB5, USB8, USB9, USB10, USB11, USB12) via USB. The PCH is connected to the CLK GEN (9LRS3199, Page 22) via 14MHz CRYSTAL. The CLK GEN provides clock signals to the PCH (133MHz, 120MHz, 100MHz, 96MHz). The PCH is connected to the DC JACK & Selector (Page 31) and the SYS POWER (Page 31). The SYS POWER is connected to various power regulators (+3V +5V UP6182, +1.5VDIMM UP6111, +VTT(1.05V) UP6111, CPU POWER ISL62882, +VCC\_GFXCORE ISL62881, +1.8VRUN APL5912KAC, CHARGER MAX8731AETI+). The PCH is connected to the ALC662 (Page 29) and the Internal SPK, Internal MIC, and Earphone (Page 30). The PCH is connected to the PCI-E LAN (RTL8103EL, Page 24) and the MINI PCIE Conn. X2 (Page 28). The PCH is connected to the HDMI (Page 11), LVDS (Page 12), and CRT (Page 12). The PCH is connected to the DC JACK & Selector (Page 31) and the SYS POWER (Page 31). The PCH is connected to the DC JACK & Selector (Page 31) and the SYS POWER (Page 31).

# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

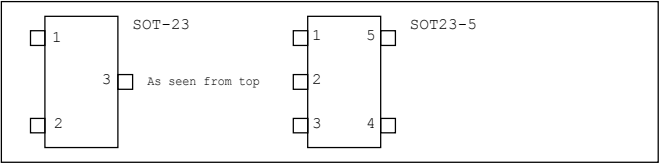
## Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0, (S3-S5)	LAN
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VSUS	3.3V	S0, (S3-S5)	
+3VRUN	3.3V	S0	DDRIII core
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	PCH DDRIII command & control pull up. CPU core rail Graphics core rail ( Dual Core only )
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V~1.1V	S0	
+VCC_GFXCORE	1.1V	S0	

## Net Naming Conventions

<b>Suffix</b>
# = Active Low Signal
<b>Prefix</b>
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

## PCB Footprints



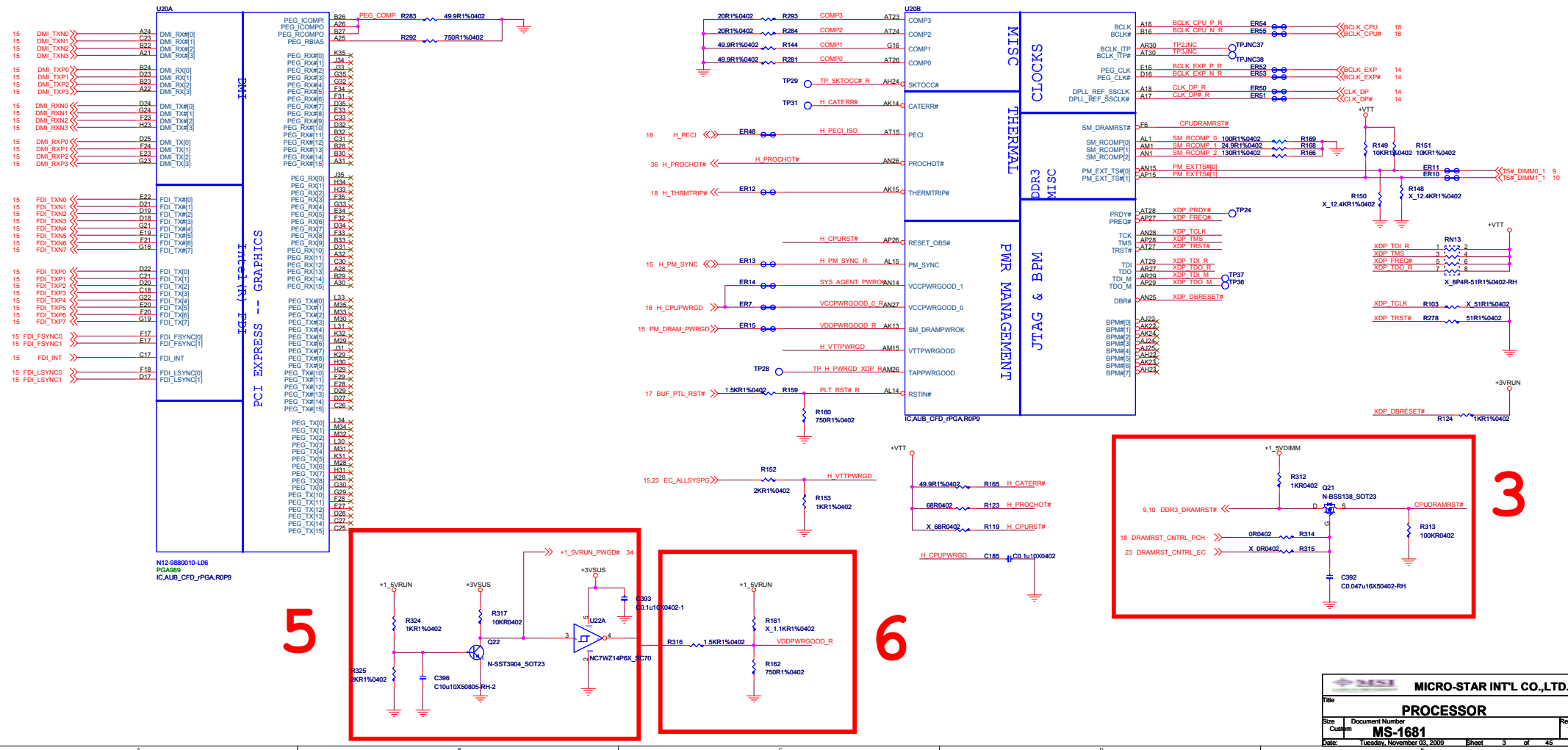
## AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

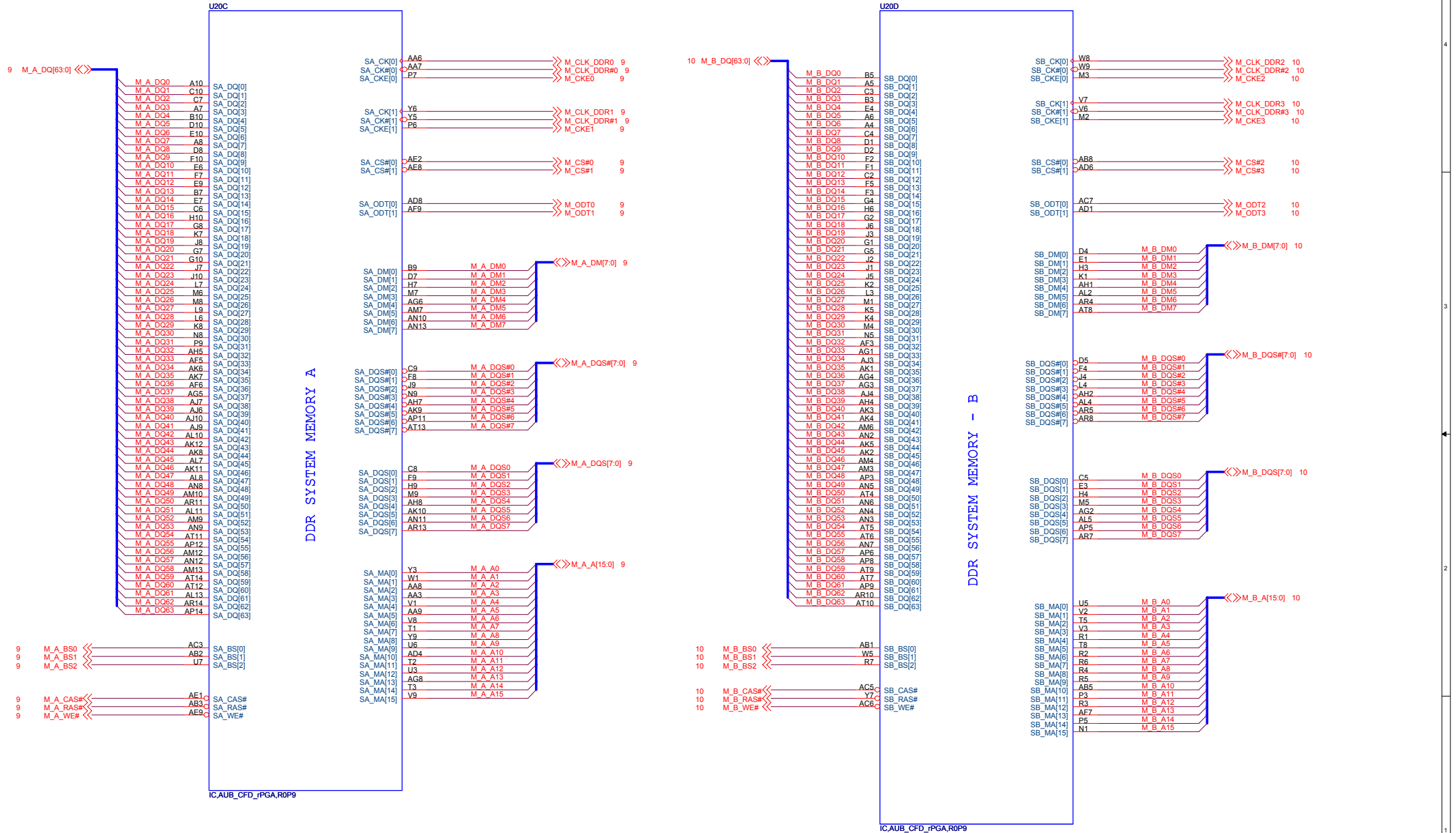
## Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

# ARRANDALE PROCESSOR (CLK,MISC,JTAG)



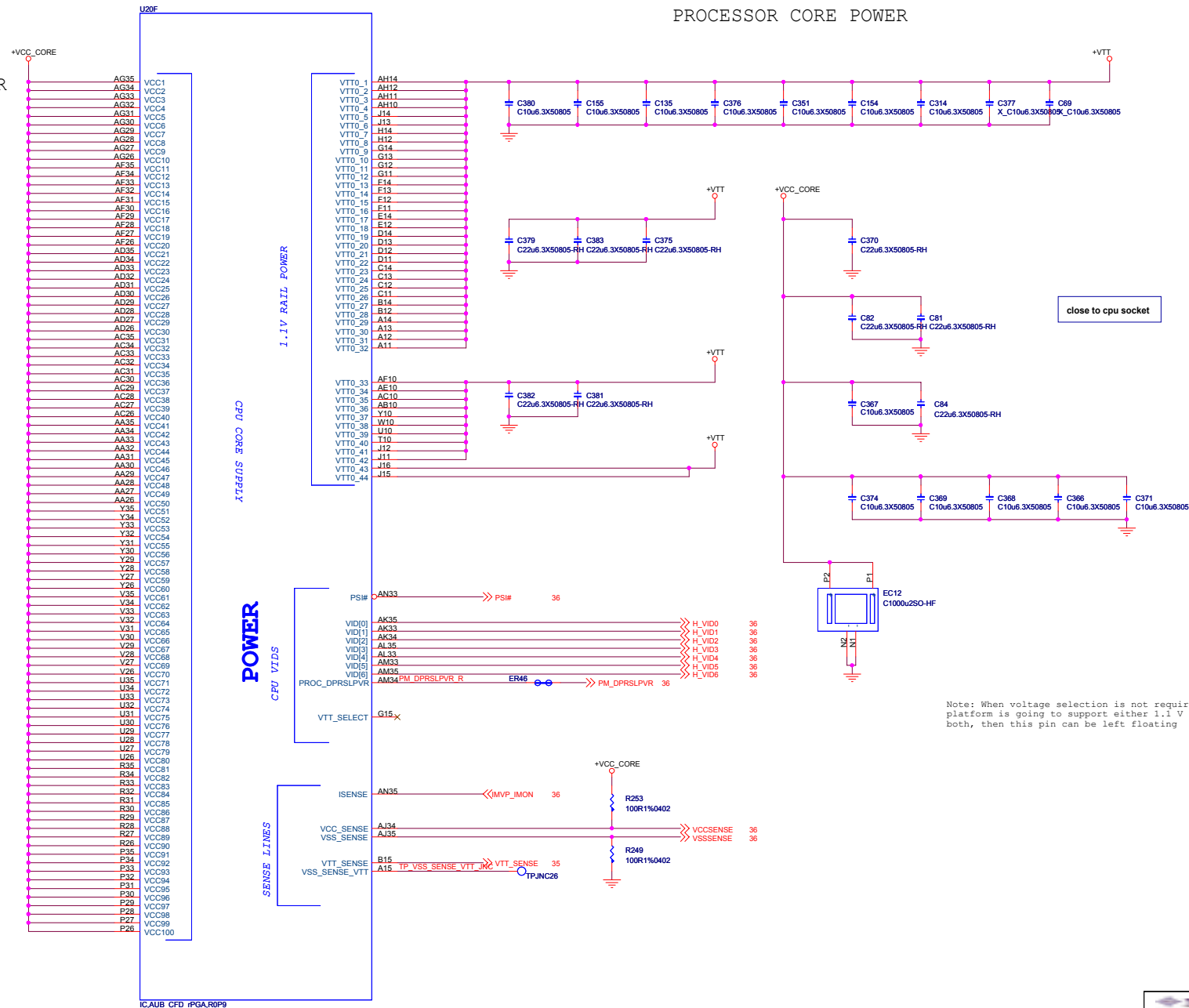
# ARRANDALE PROCESSOR (DDR3)



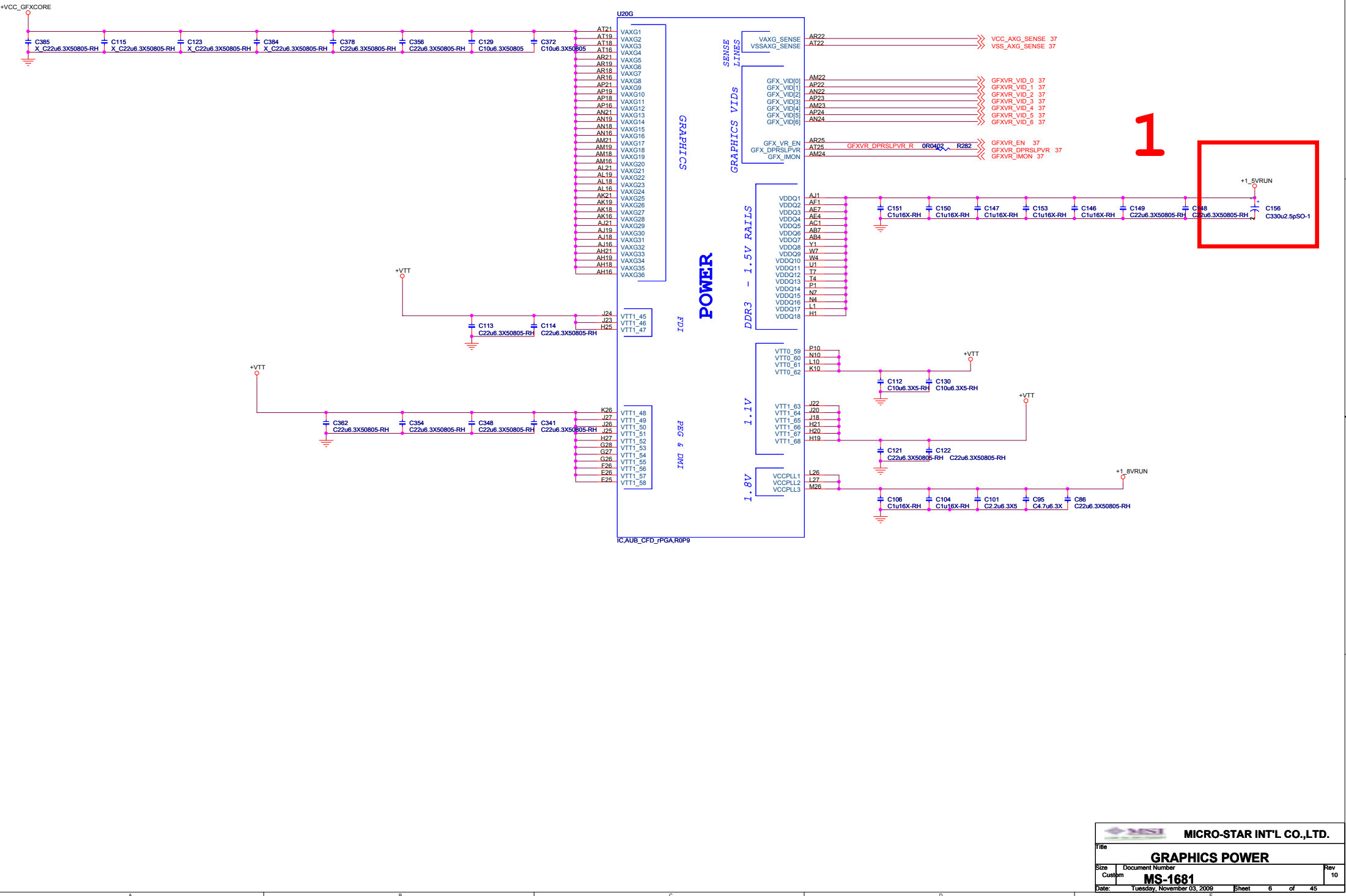
# ARRANDALE PROCESSOR (POWER)

PROCESSOR CORE POWER

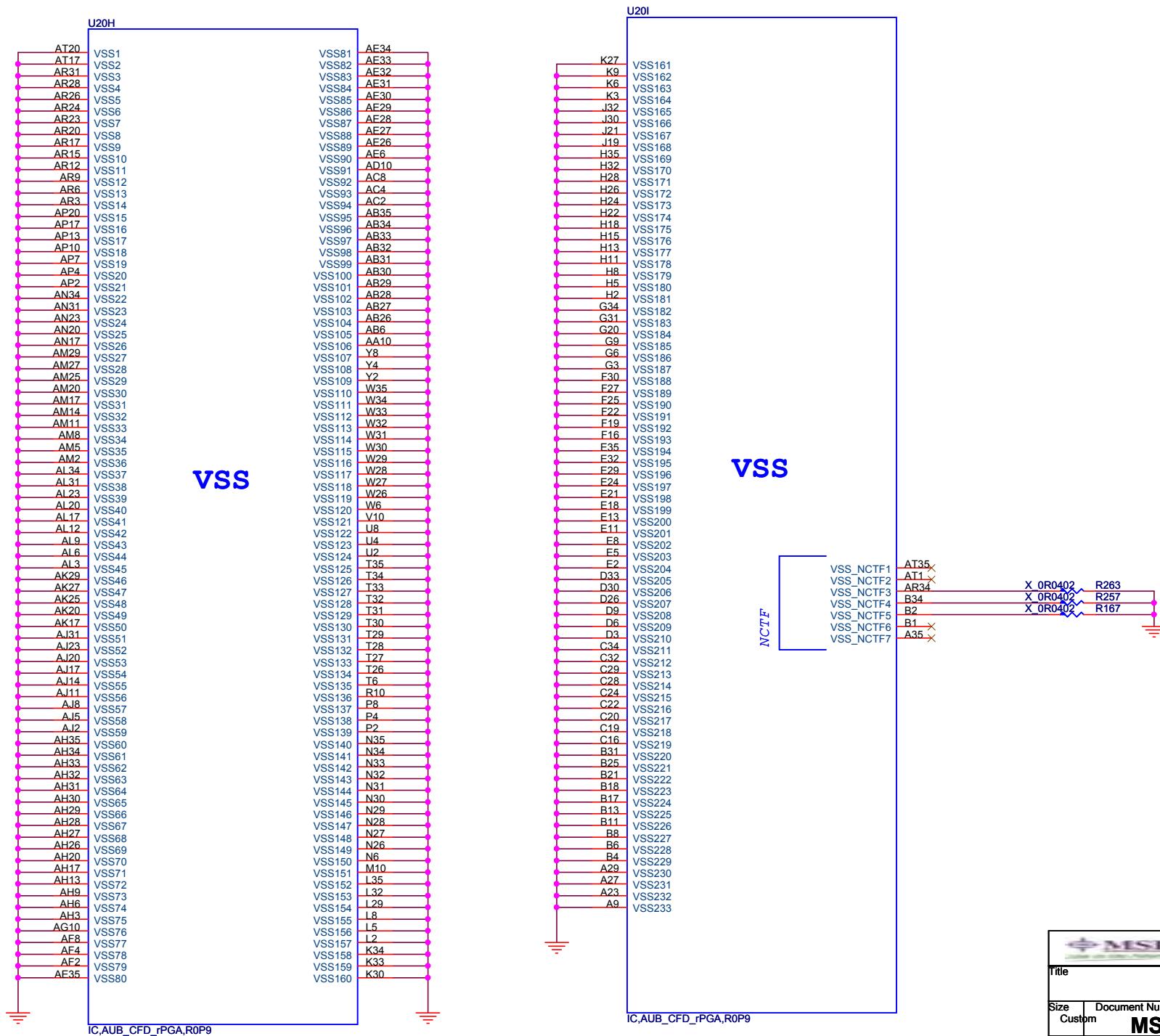
PROCESSOR CORE POWER



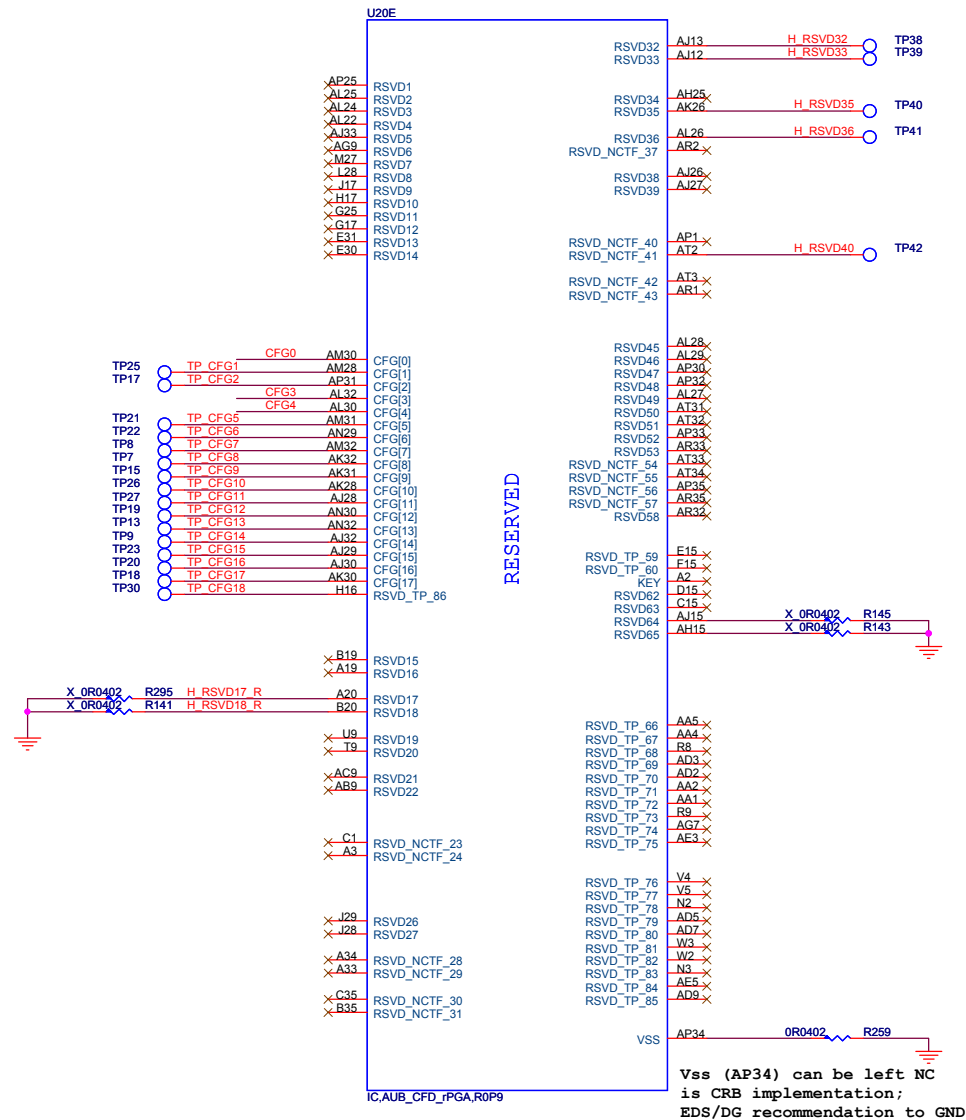
ARRANDALE PROCESSOR (GRAPHICS POWER)



# ARRANDALE PROCESSOR (GND)



## ARRANDALE PROCESSOR (RESERVED)



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

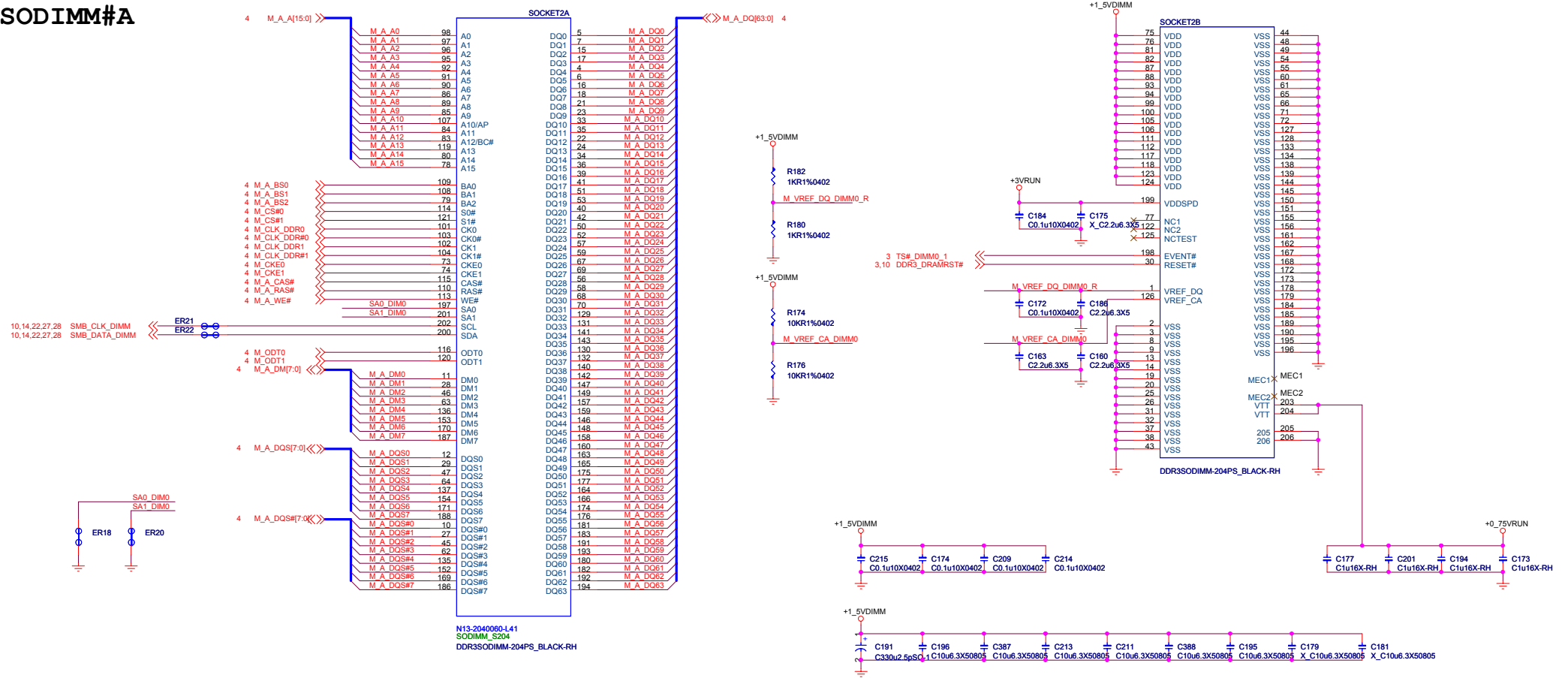
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	<p>1:Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0:Enabled; An external Display Port device is connected to the Embedded Display Port</p>

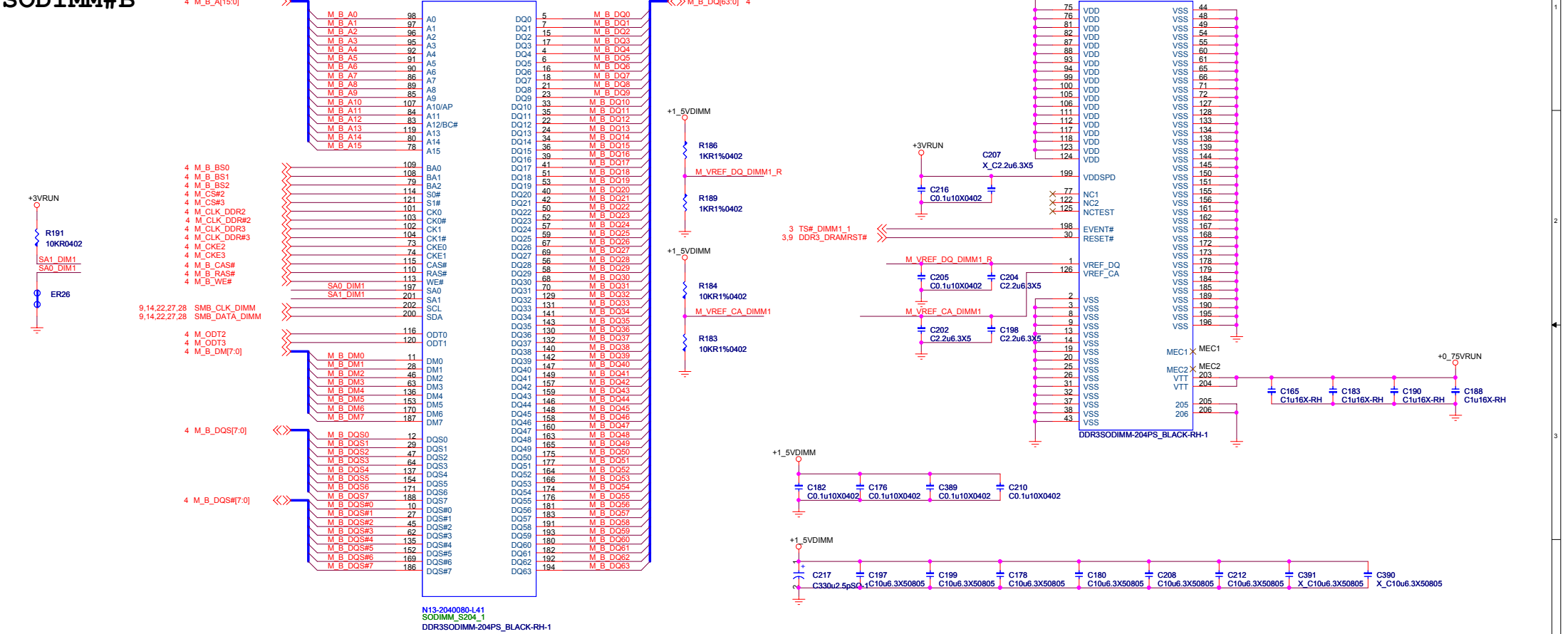
Layout Note:  
Location of all CFG strap resistors needs  
to be close to trace to minimize stub




SODIMM#A



SODIMM#B



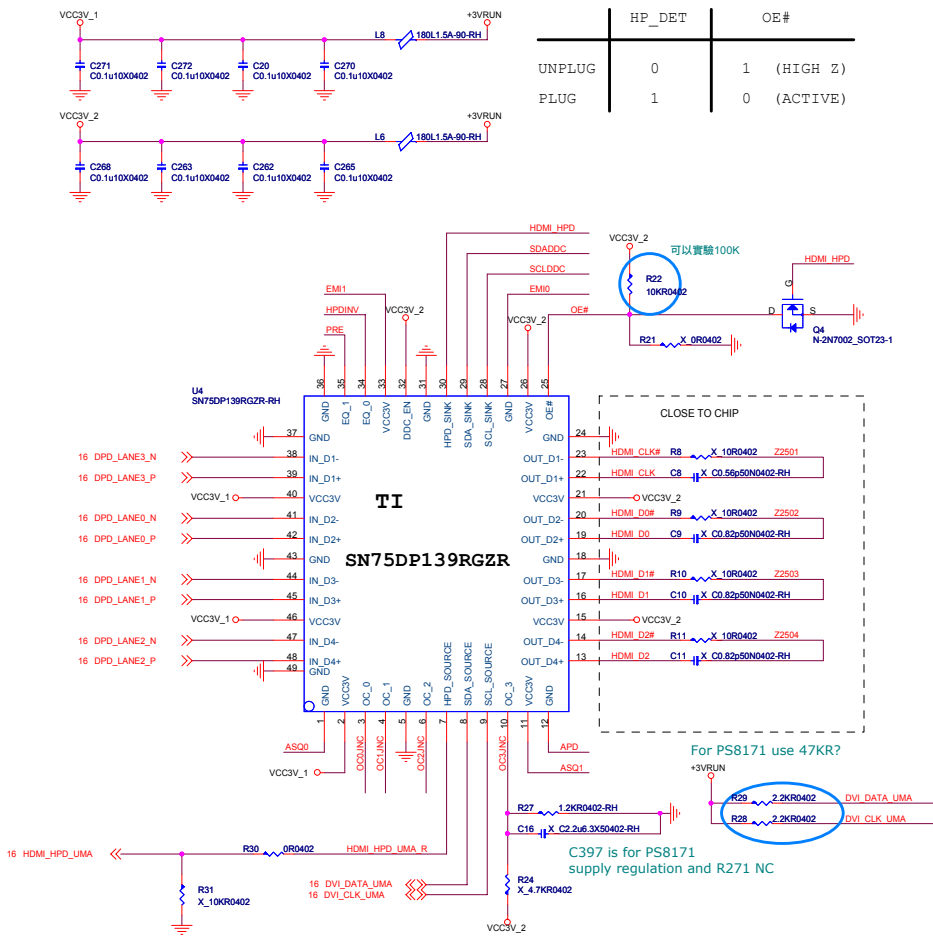
**MICRO-STAR INT'L CO.,LTD.**

**DDR3 SODIMM1**

Size	Document Number	Rev
Custom	<b>MS-1681</b>	10

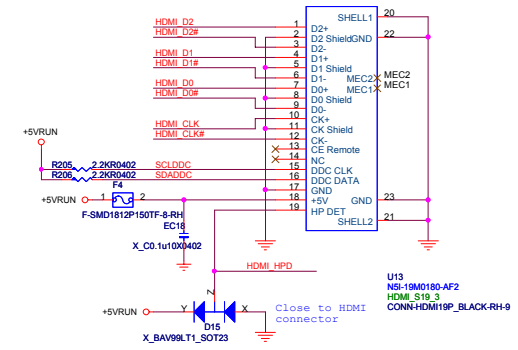
Date:	Tuesday, November 03, 2009	Sheet	10	of	45
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# HDMI Switch



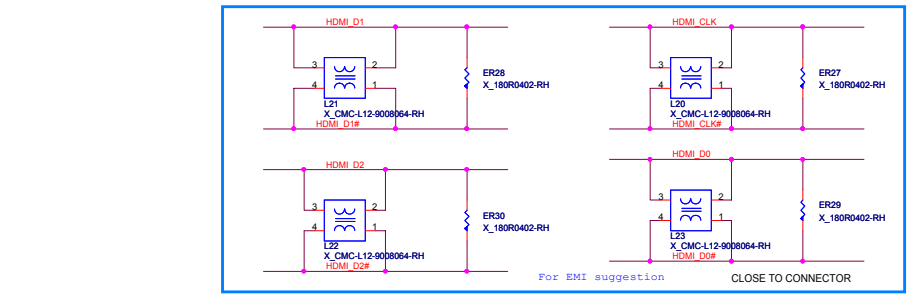
	HP_DET	OE#
UNPLUG	0	1 (HIGH Z)
PLUG	1	0 (ACTIVE)

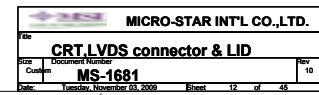
## HDMI connector



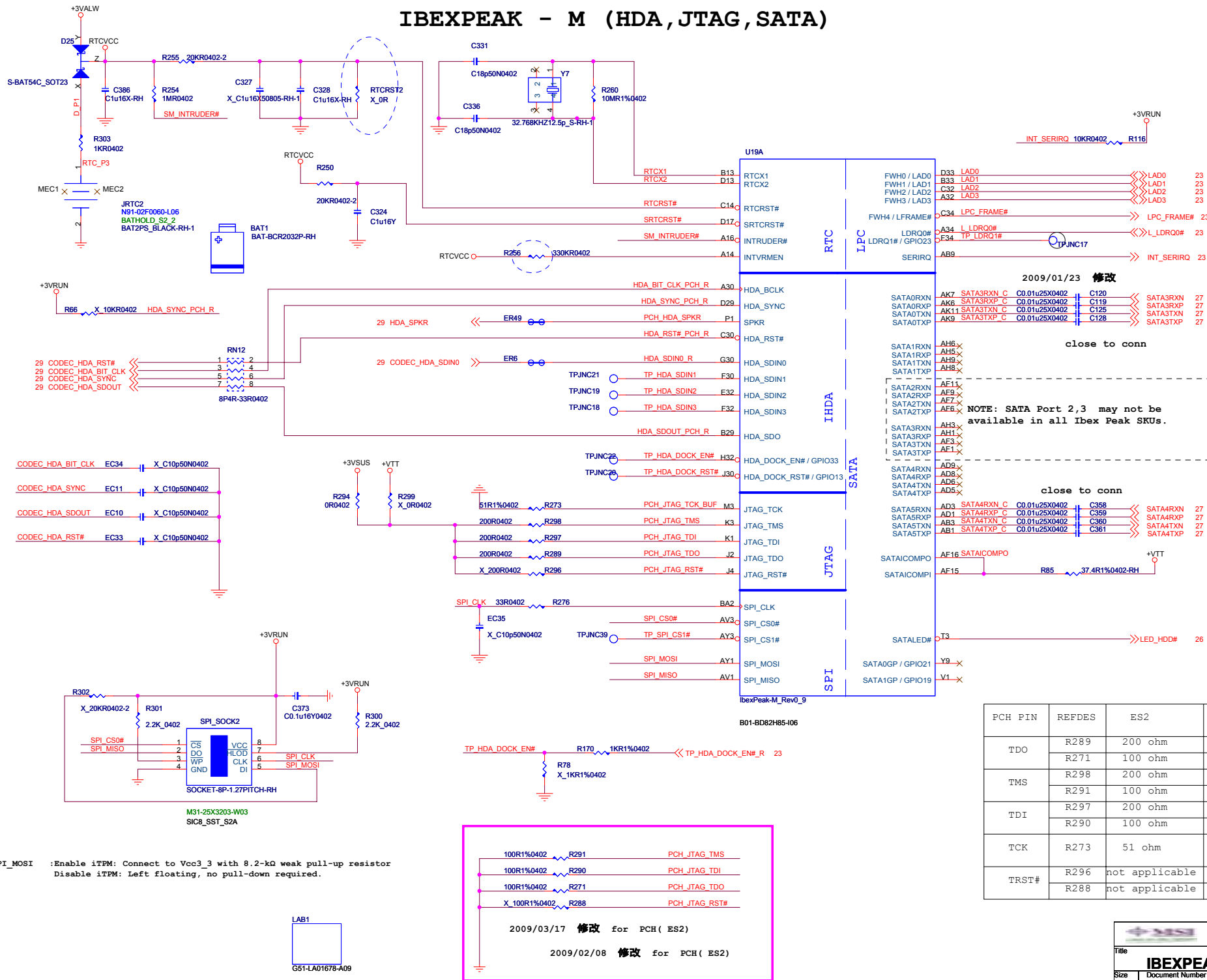
SN75DP139	PS8171	Pin no.
Floating	TMDS inputs equalization control (internal pull-down~500K) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ	Pin 3
High	(Internal pull down~500K) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD = HPD_SINK# (inverted HPD) @ 0.9V	Pin 4
GND	[ASQ1.ASQ0] = HL: No automatic squelch (Internal pull down~500K) LL: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1 Pin 11
4.65K to GND	499R to GND	Pin 6
GND	Automatic power down management (Internal pull up~500K) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND	EMI reduction and filter setting: (EMI1 internal pull up~500K; EMI0 internal pull down~500K) [EMI1,EMI0] = HL: No EMI reduction EMI0 = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27 Pin 33
Note2	DDC Active Buffer enable and setting (internal pull-down~500K) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2	Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down~500K) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added	Pin 35

Note2: High is HPD logic inverted, Low is HPD logic non-inverted



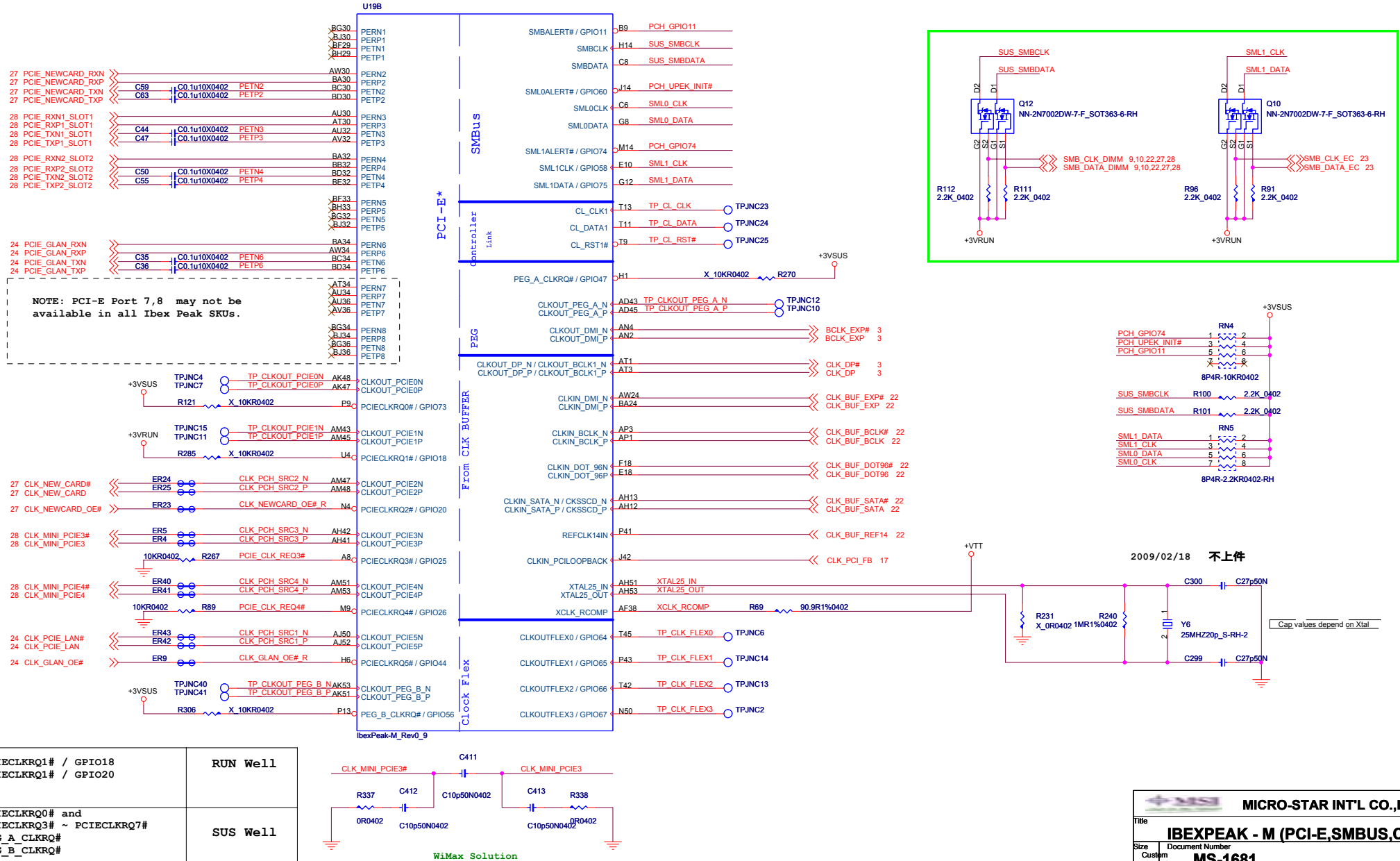


# IBEXPEAK - M (HDA, JTAG, SATA)



PCH PIN	REFDES	ES2	STATE
TDO	R289	200 ohm	STUFF
	R271	100 ohm	STUFF
TMS	R298	200 ohm	STUFF
	R291	100 ohm	STUFF
TDI	R297	200 ohm	STUFF
	R290	100 ohm	STUFF
TCK	R273	51 ohm	STUFF
TRST#	R296	not applicable	NO STUFF
	R288	not applicable	NO STUFF

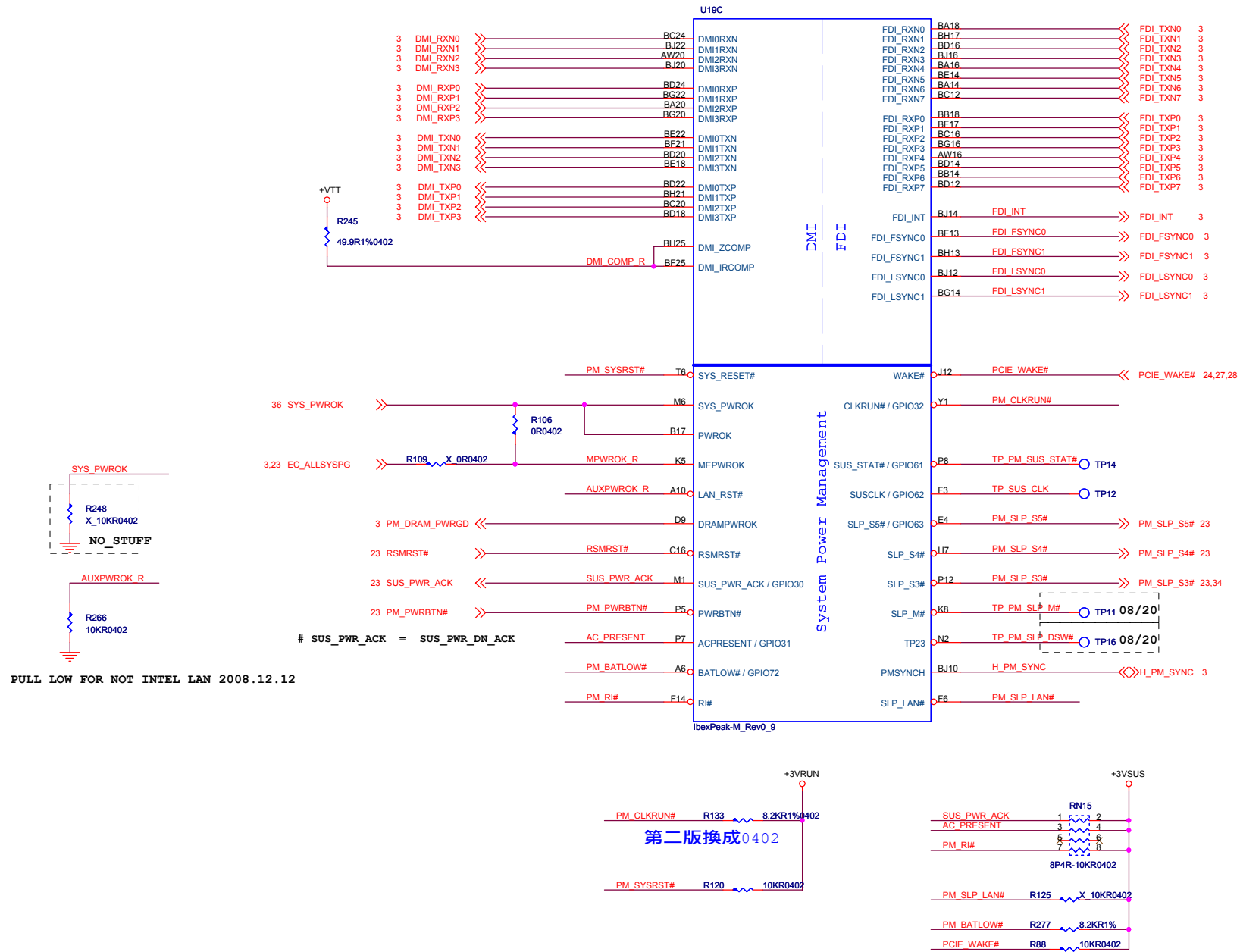
# IBEXPEAK - M (PCI-E, SMBUS, CLK)



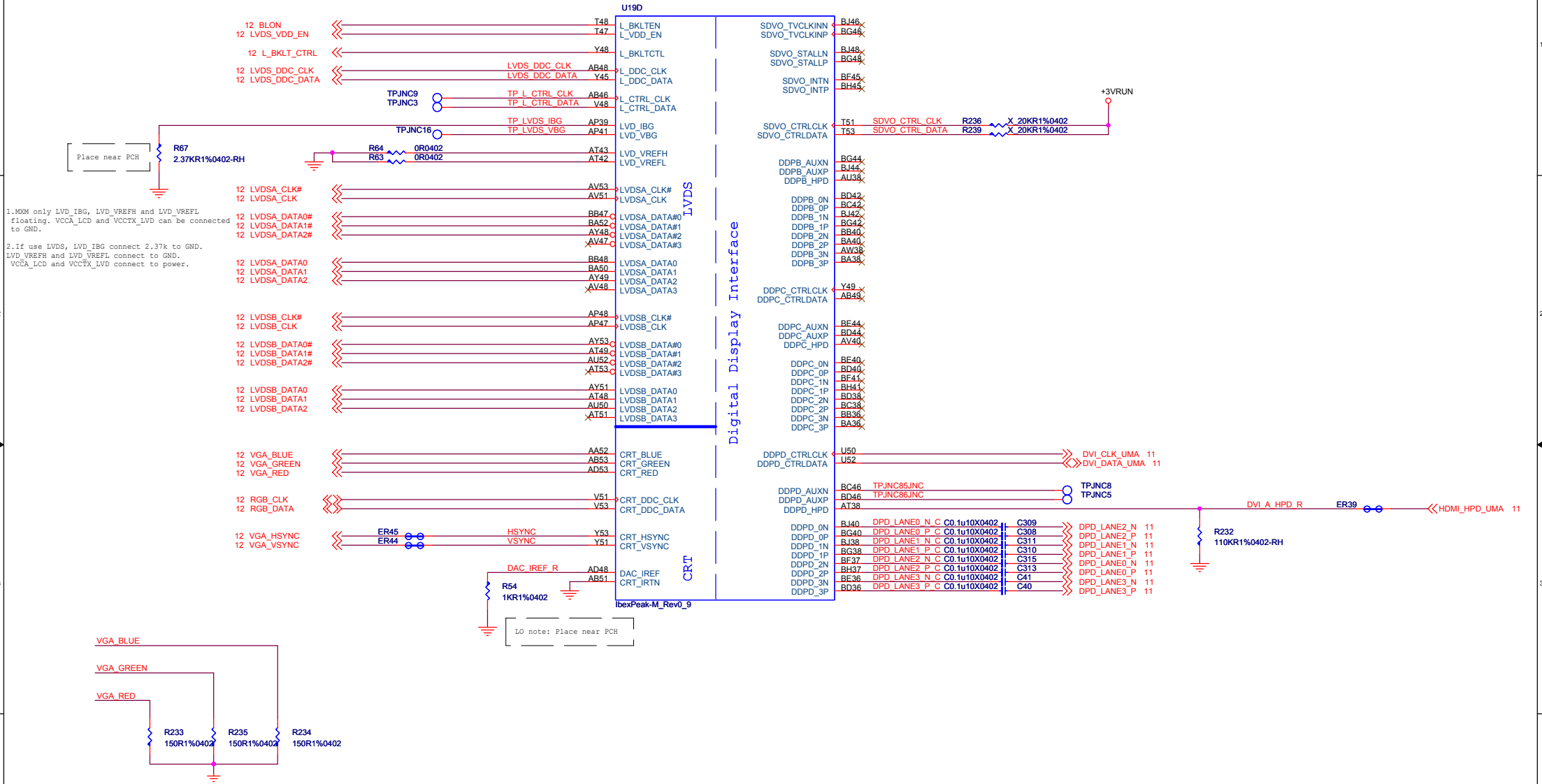
PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

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IBEXPEAK - M (PCI-E,SMBUS,CLK)			
Size	Document Number	Rev	
Custom	MS-1681	10	
Date:	Tuesday, November 03, 2009	Sheet	14 of 45

## IBEXPEAK - M (DMI, FDI, GPIO)



# IBEXPEAK - M (LVDS,DDI)

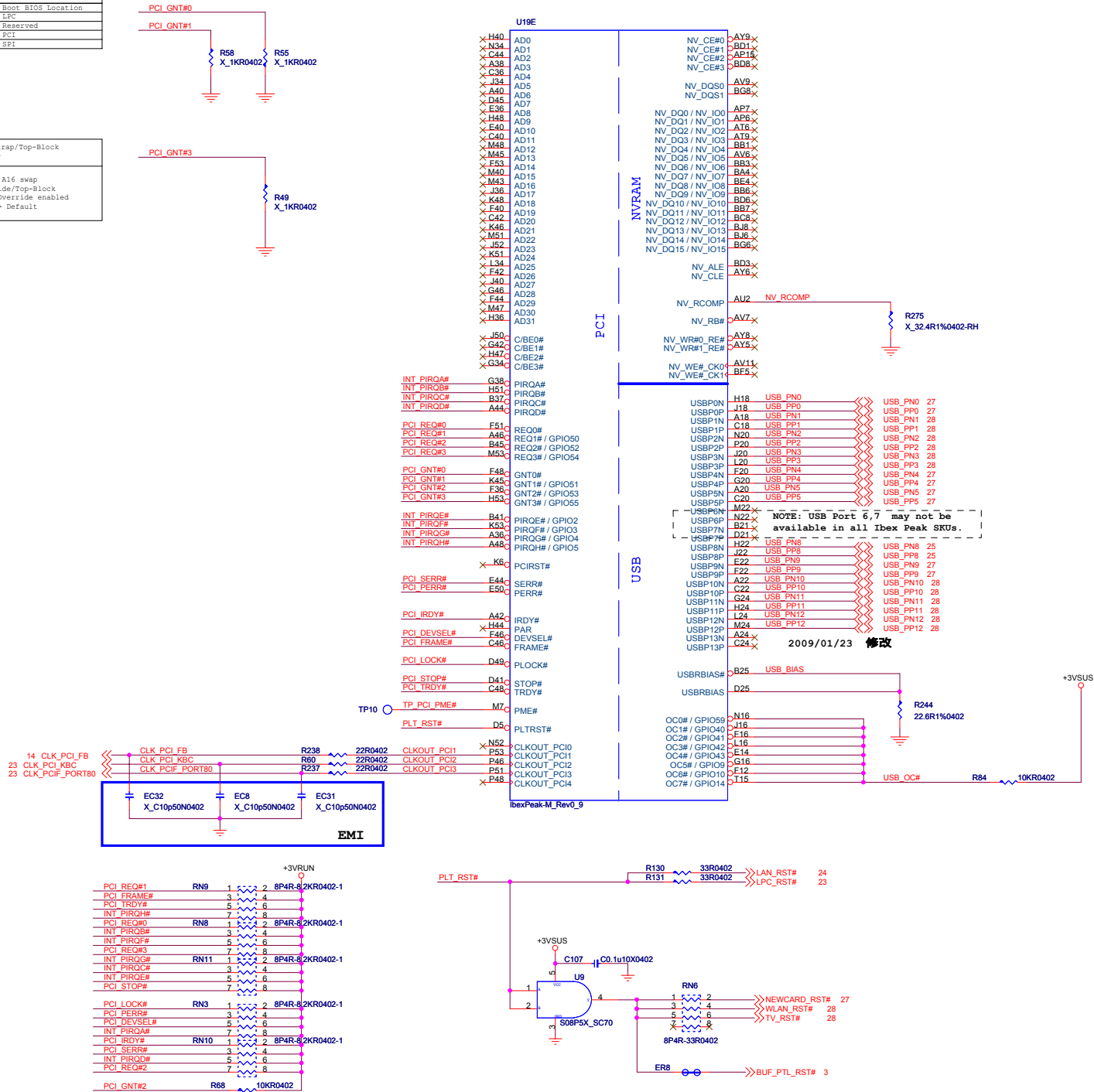




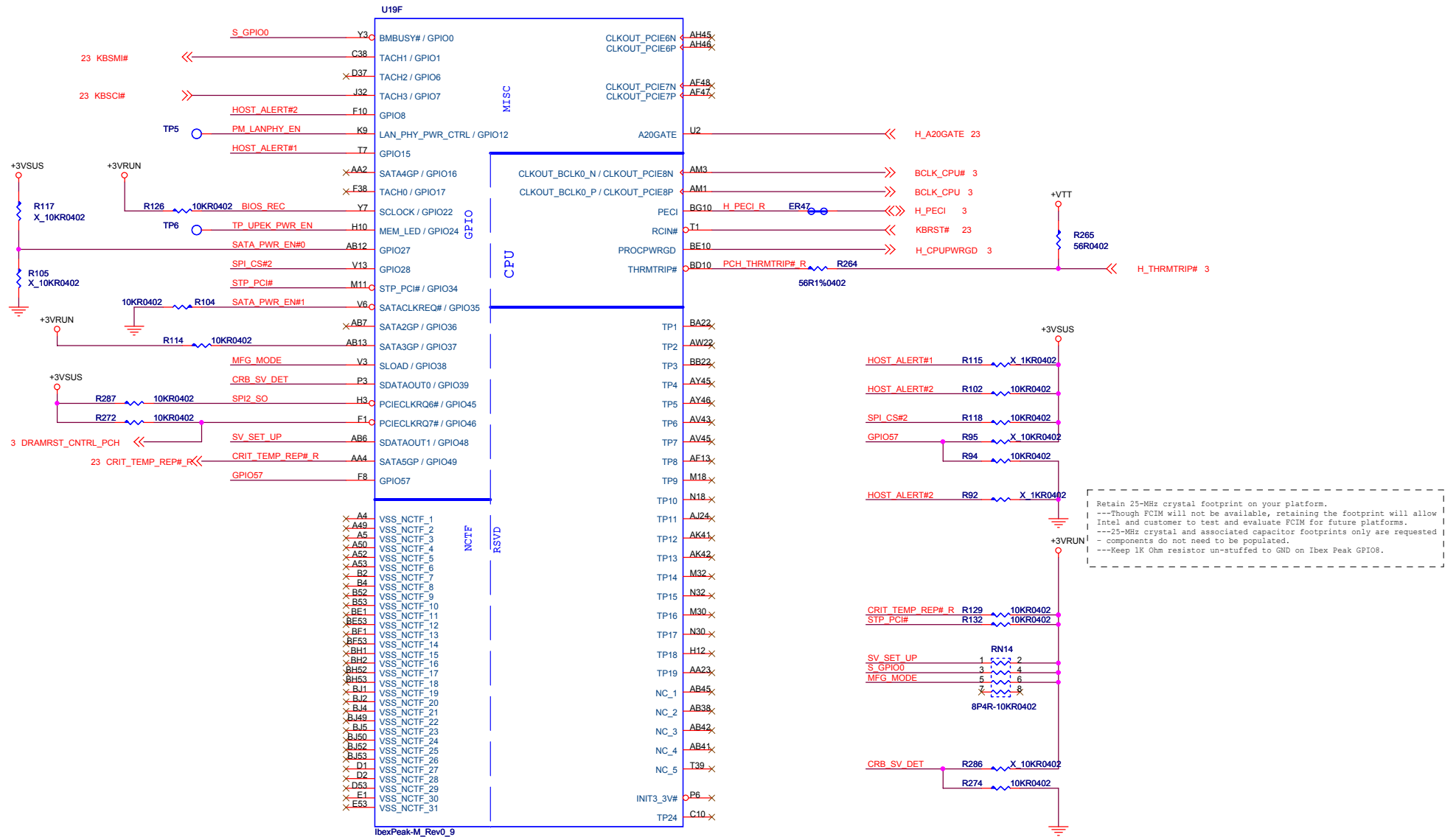
# IBEXPEAK - M (PCI,USB,NVRAM)

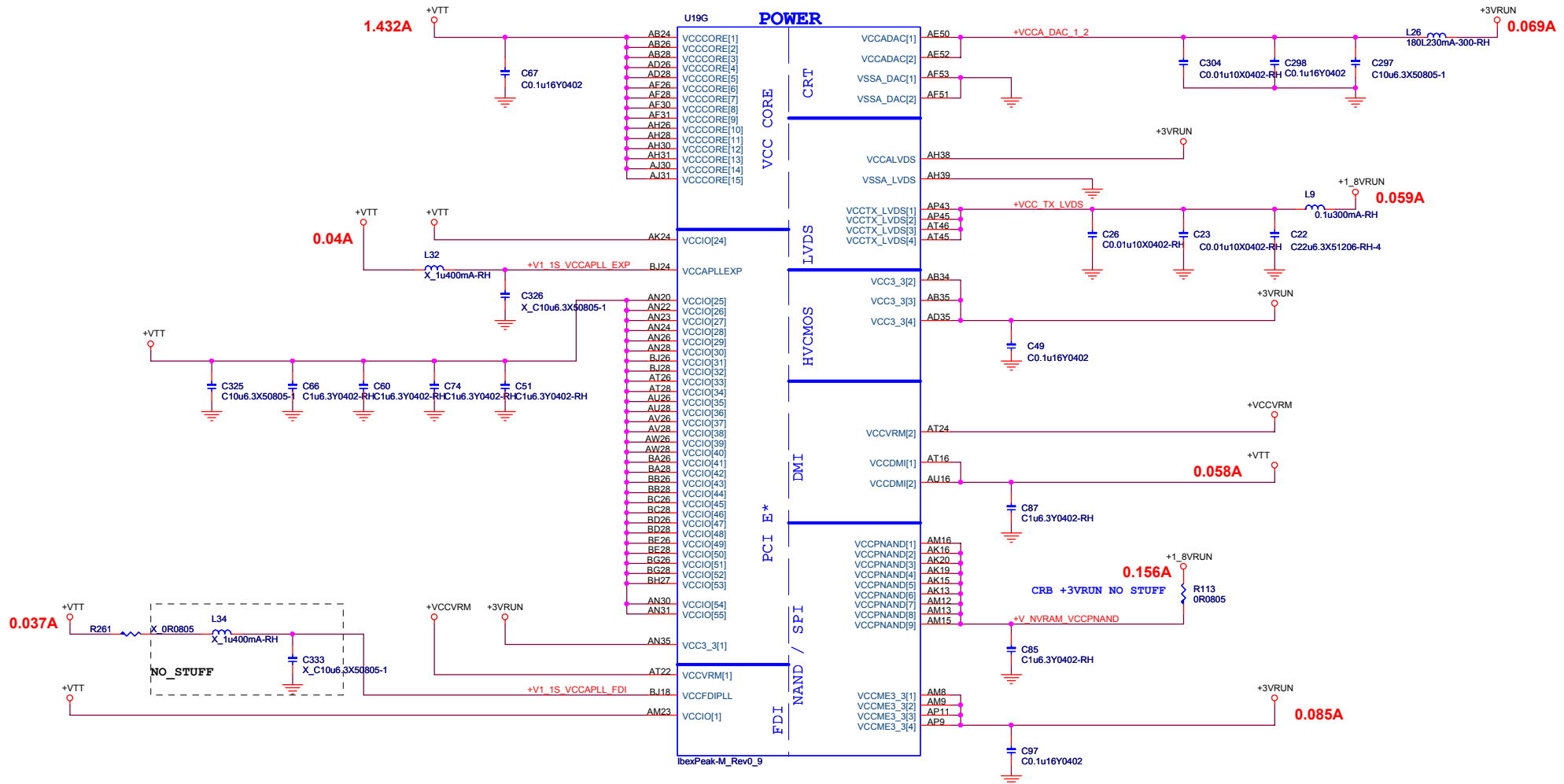
Boot BIOS Strap		
PCI GNT#0	PCI GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPi

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

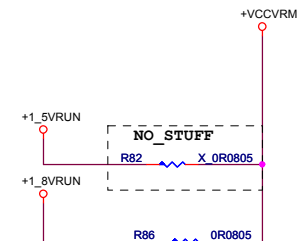


# IBEXPEAK - M (GPIO,VSS\_NCTF,RSVD)

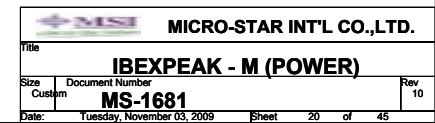


**IBEXPEAK - M (POWER)**

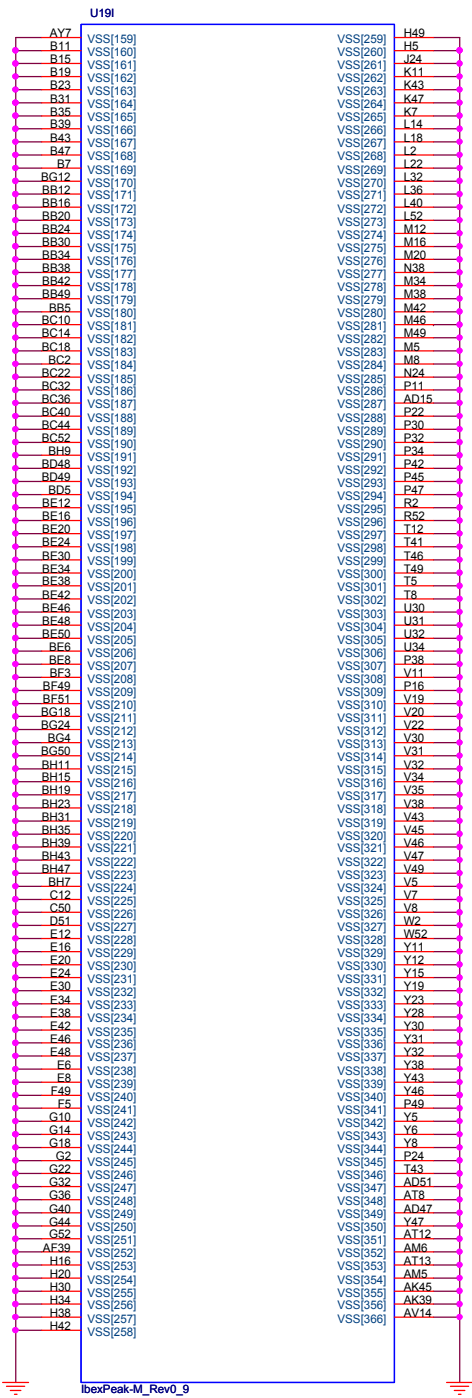
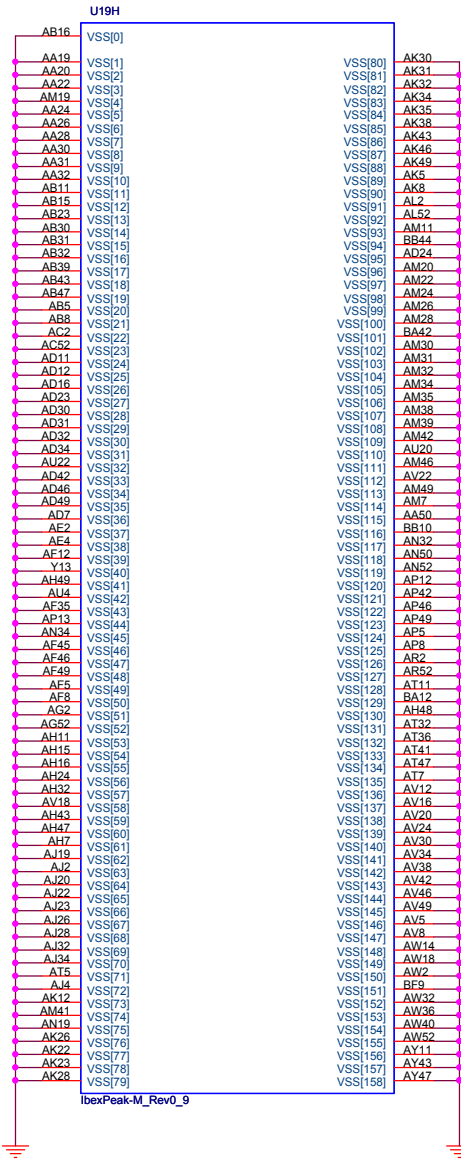
The VCCVRM rail (1.8 v/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAclk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

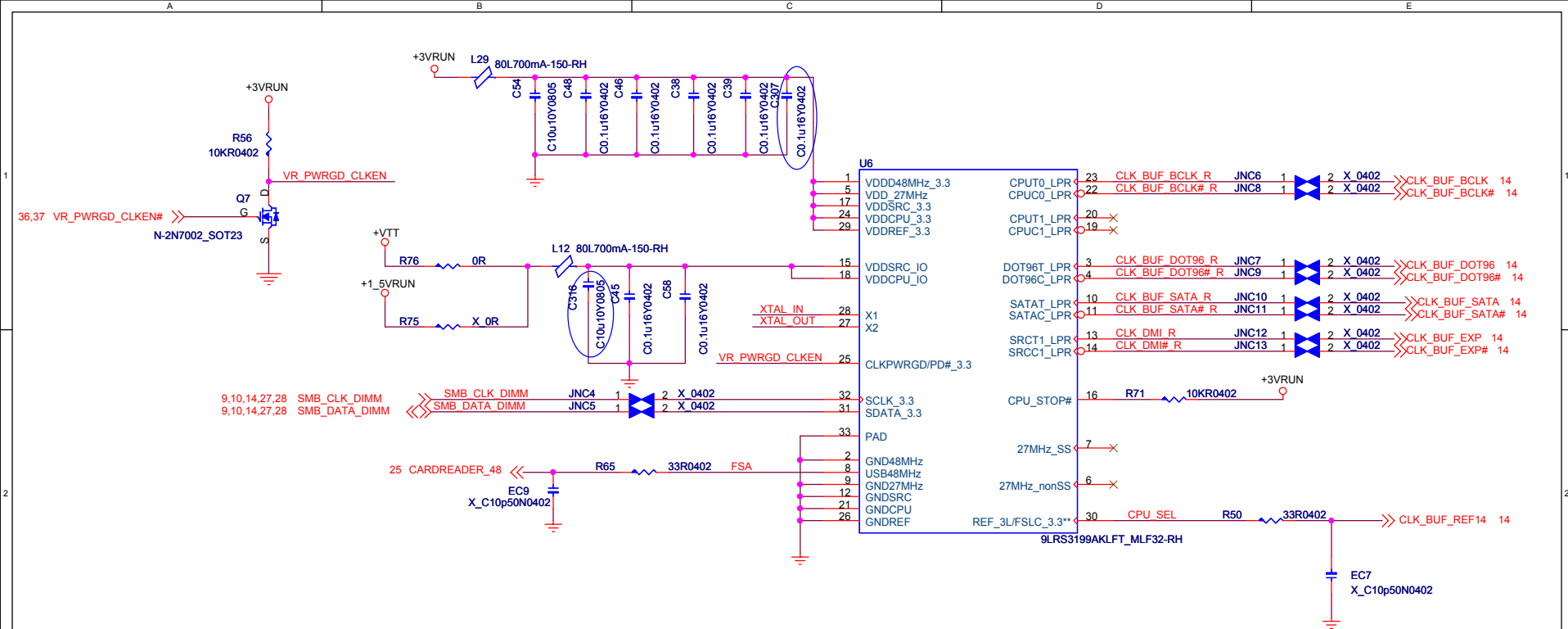


IBEXPEAK - M (POWER)



IBEXPEAK - M (GND)

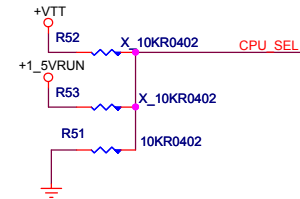
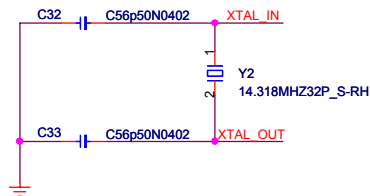




For CPU frequency select (133MHz)

### Capacity select

If LC=20pf C708/C709=33pf  
If LC=32pf C708/C709=56pf

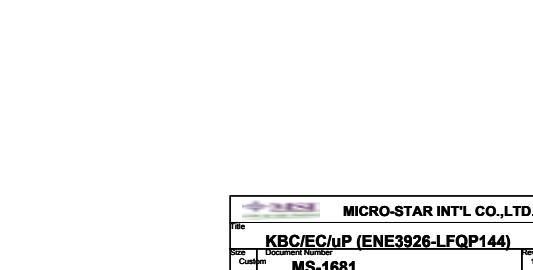
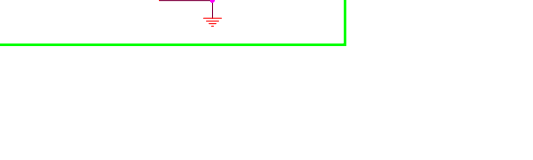
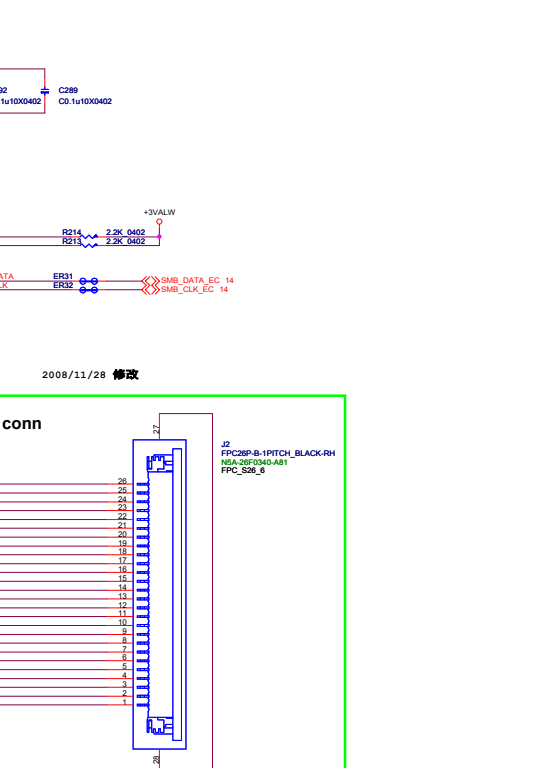
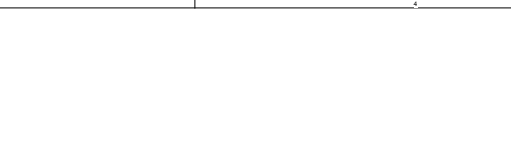
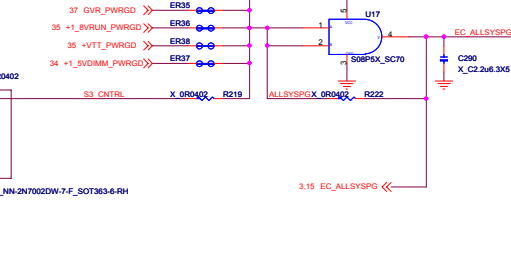
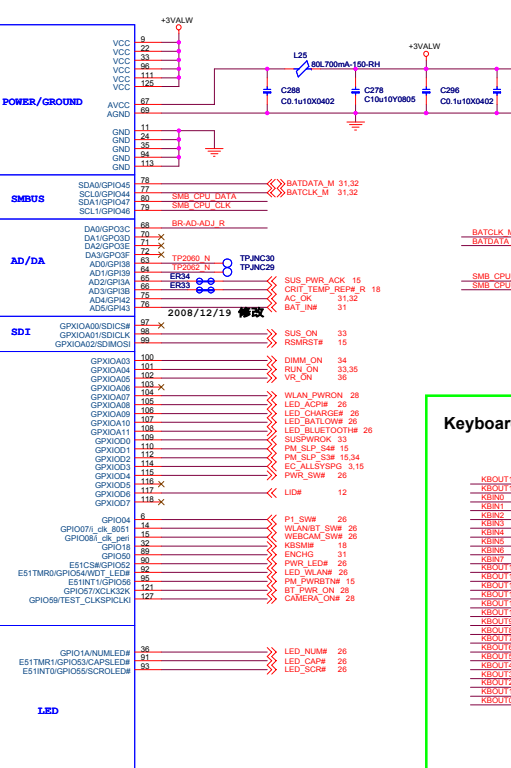
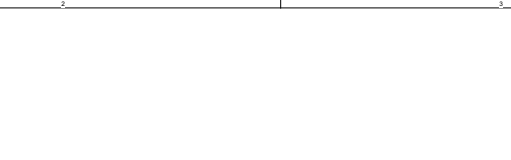
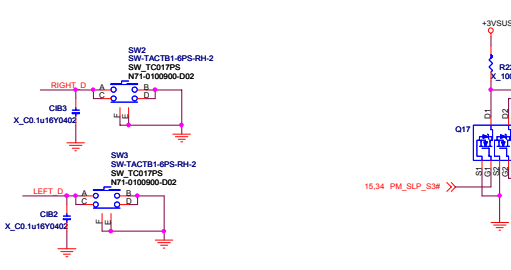
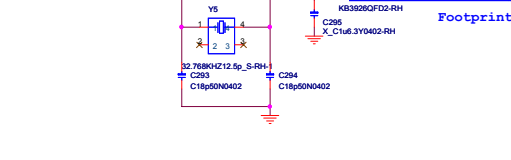
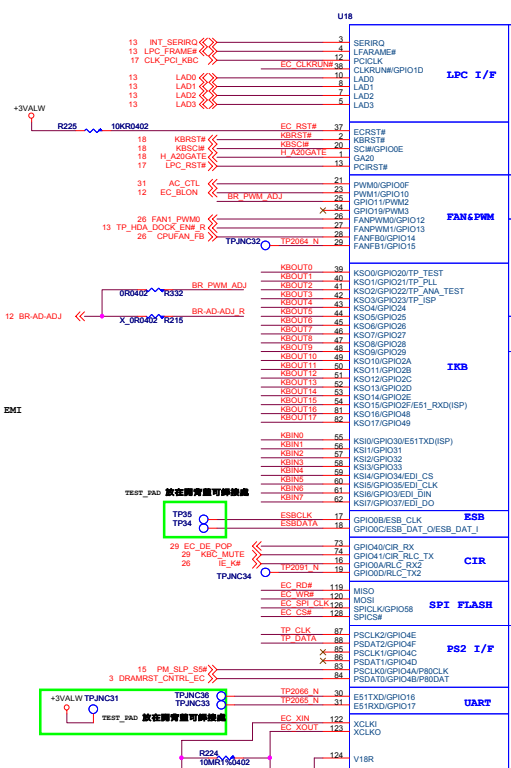
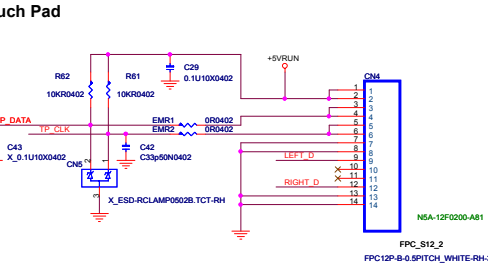
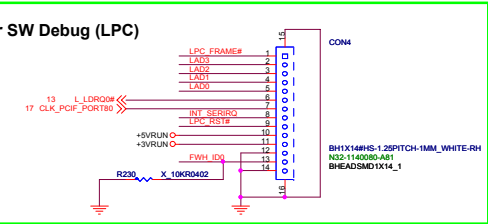
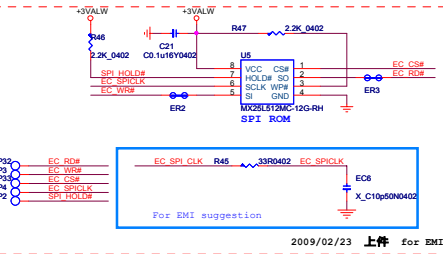
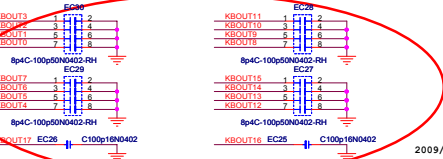
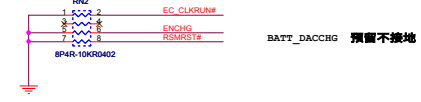
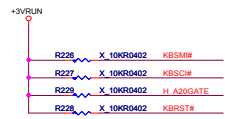


CPU_SEL	CPU0	CPU1
0 (Default)	133MHz	133MHz
1 (1.05~1.5V)	100MHz	100MHz

### Co-Lay Note:

For IDT IC91RS3199  
R598,R599,R600=10Kohm

For Silago SLG8SP587  
R598,R599,R600=4.7Kohm



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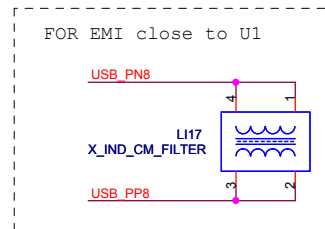
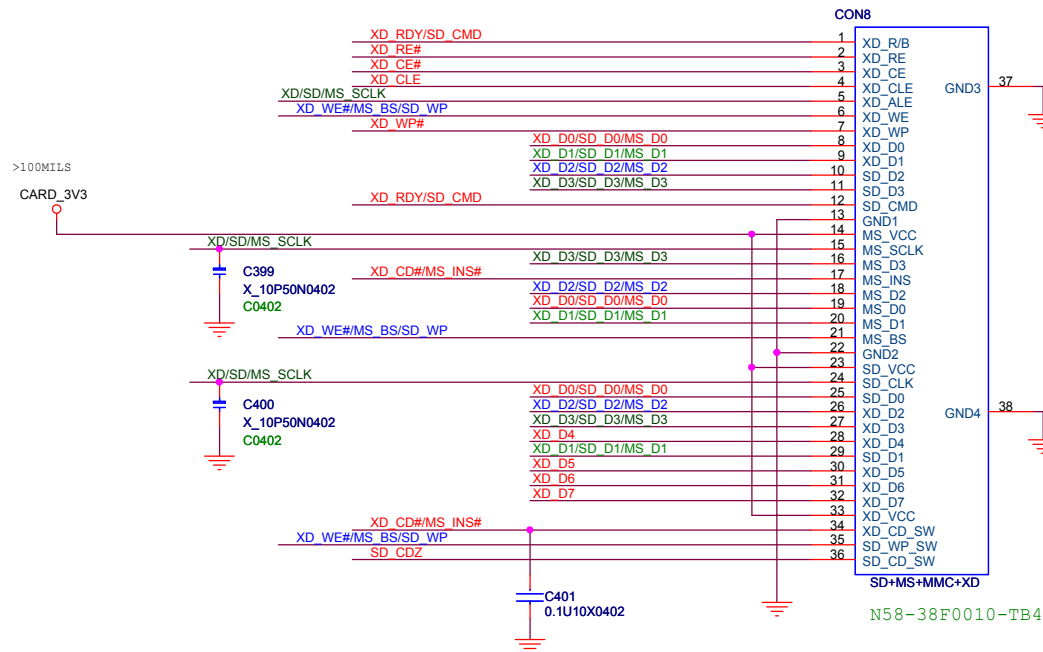
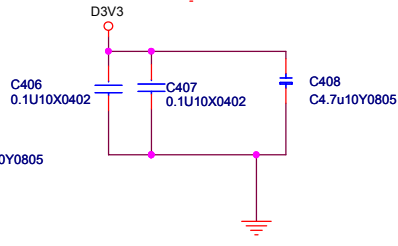
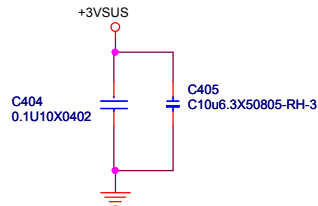
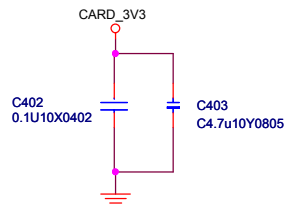
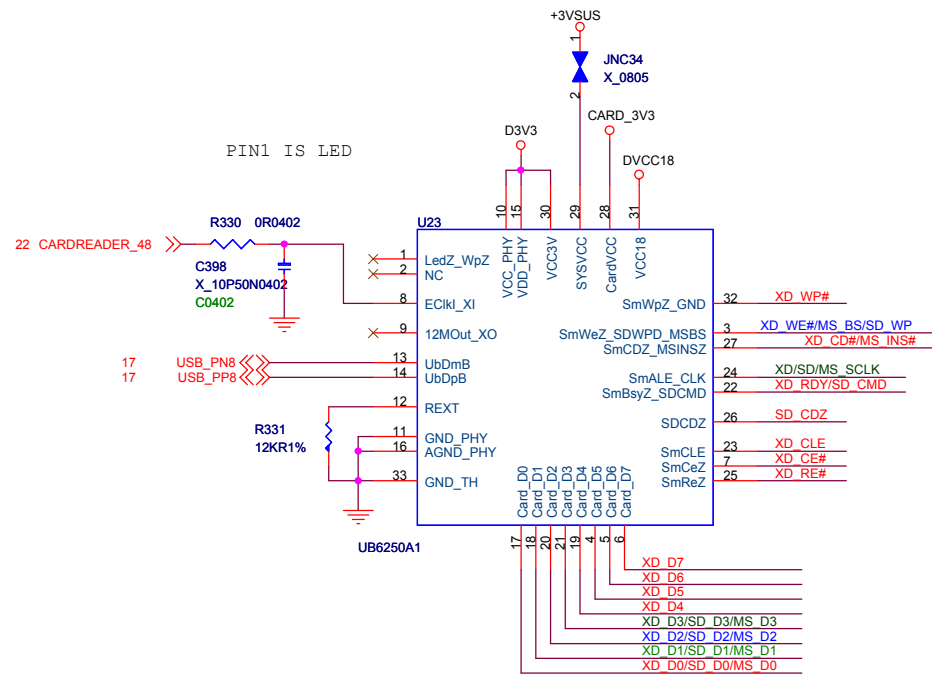


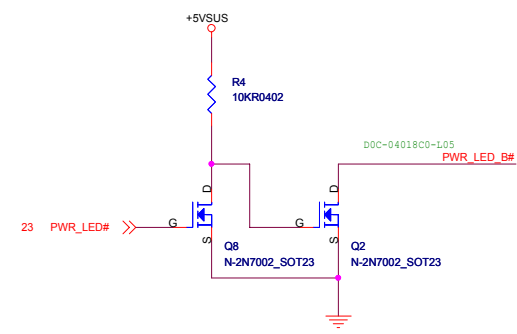
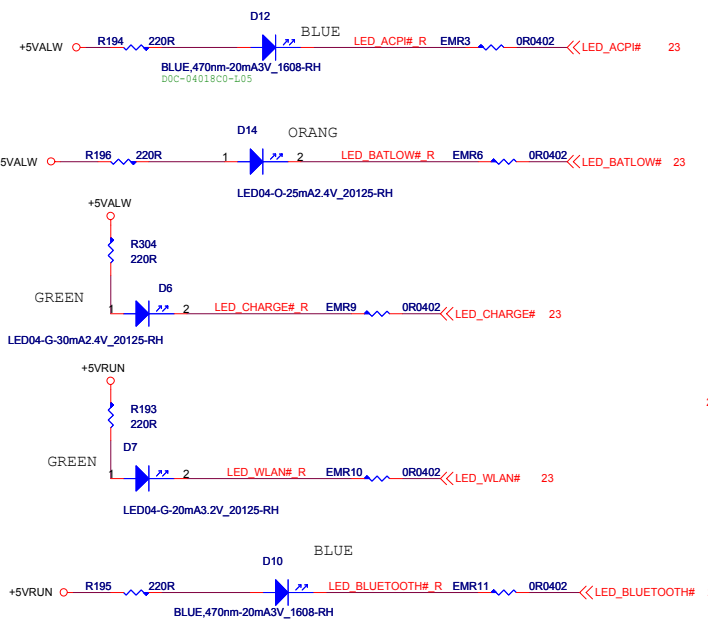
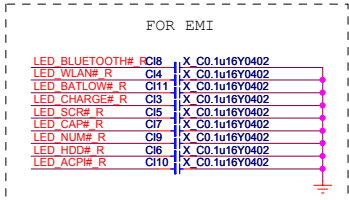
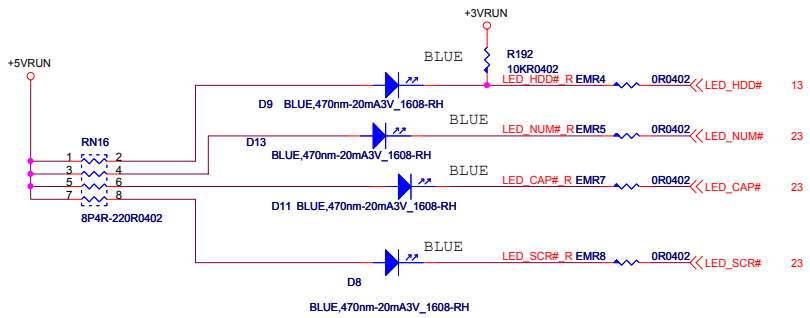
## 3

4

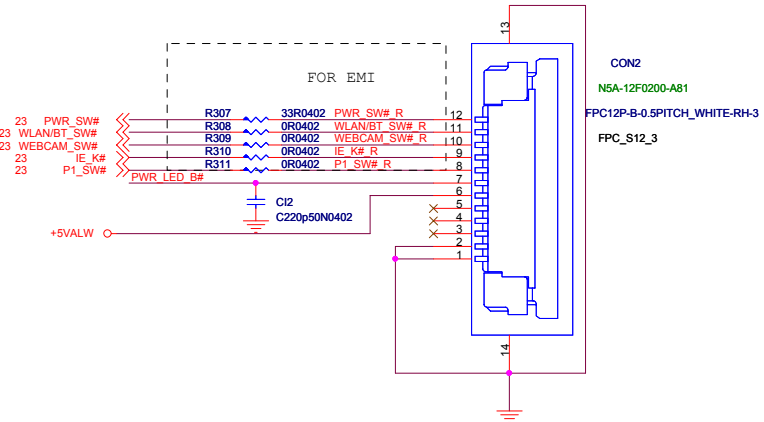
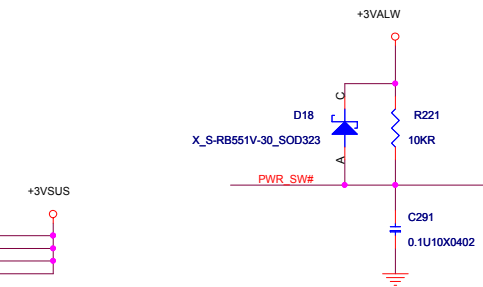
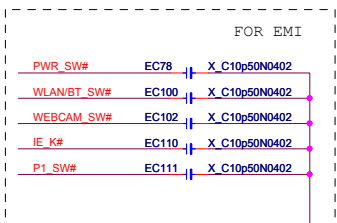
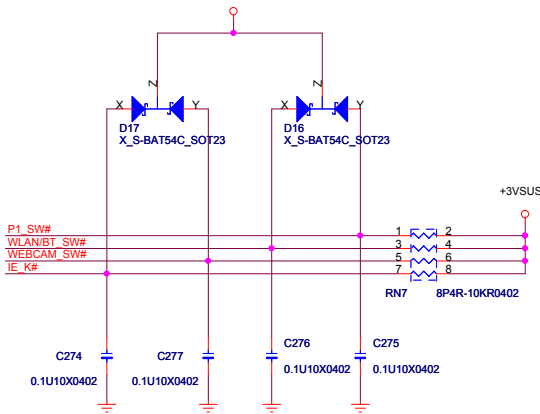
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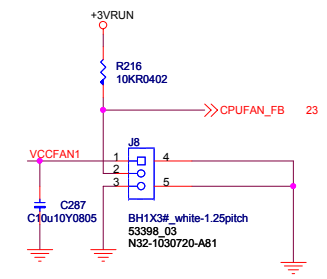
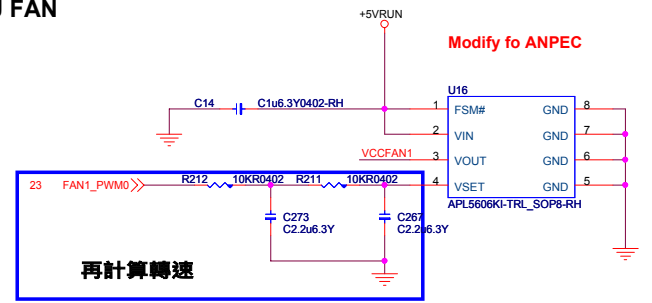




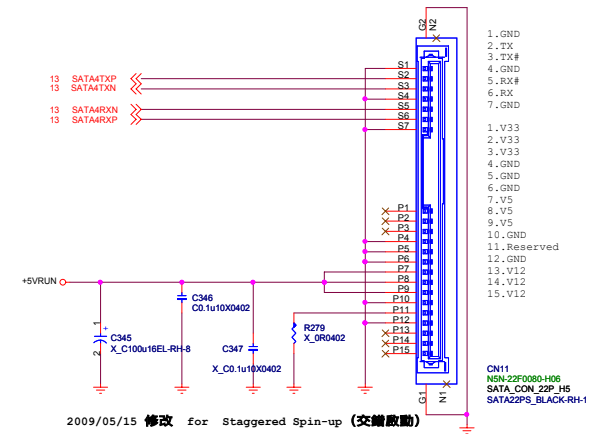
# CLOSE TO CONNECTOR



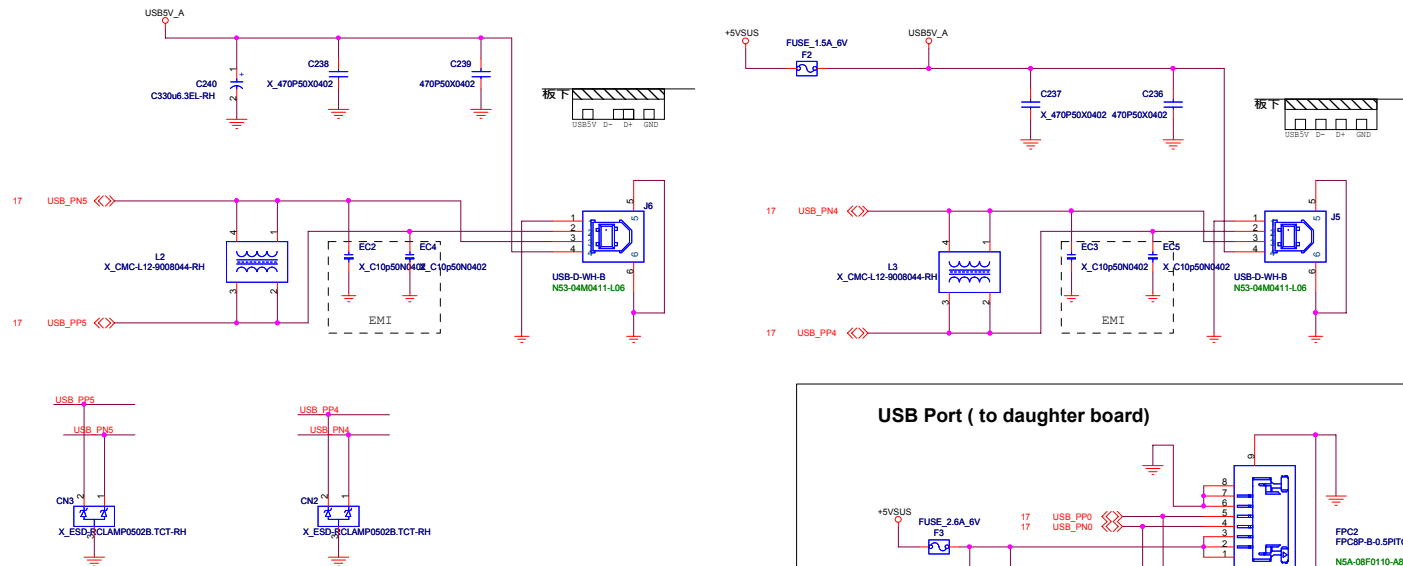
# CPU FAN



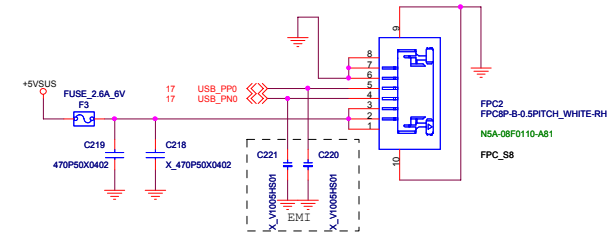
## SATA HDD



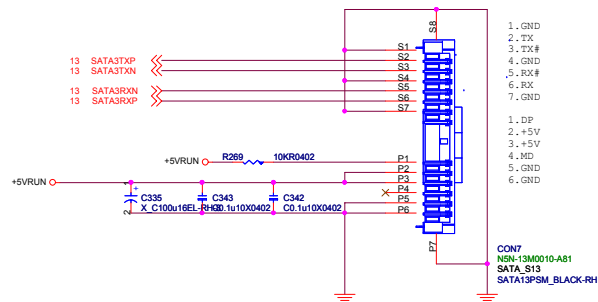
## USB Port



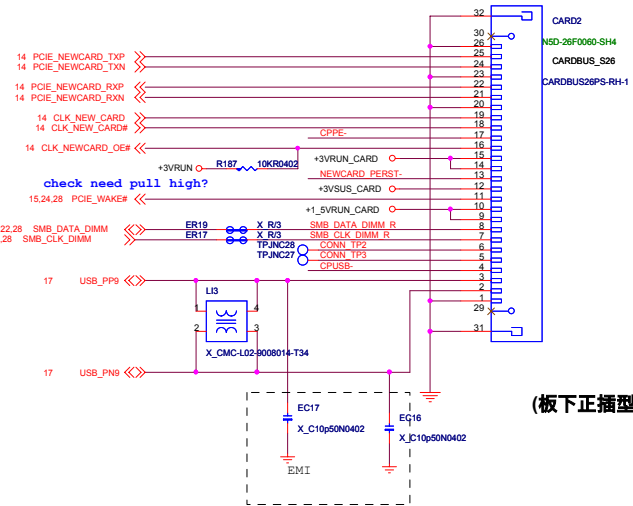
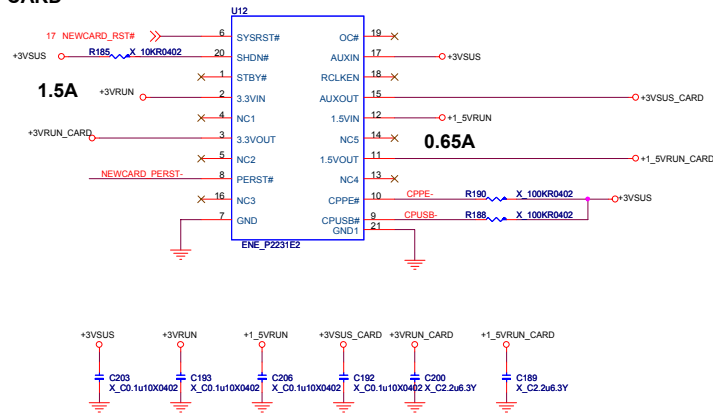
## USB Port (to daughter board)



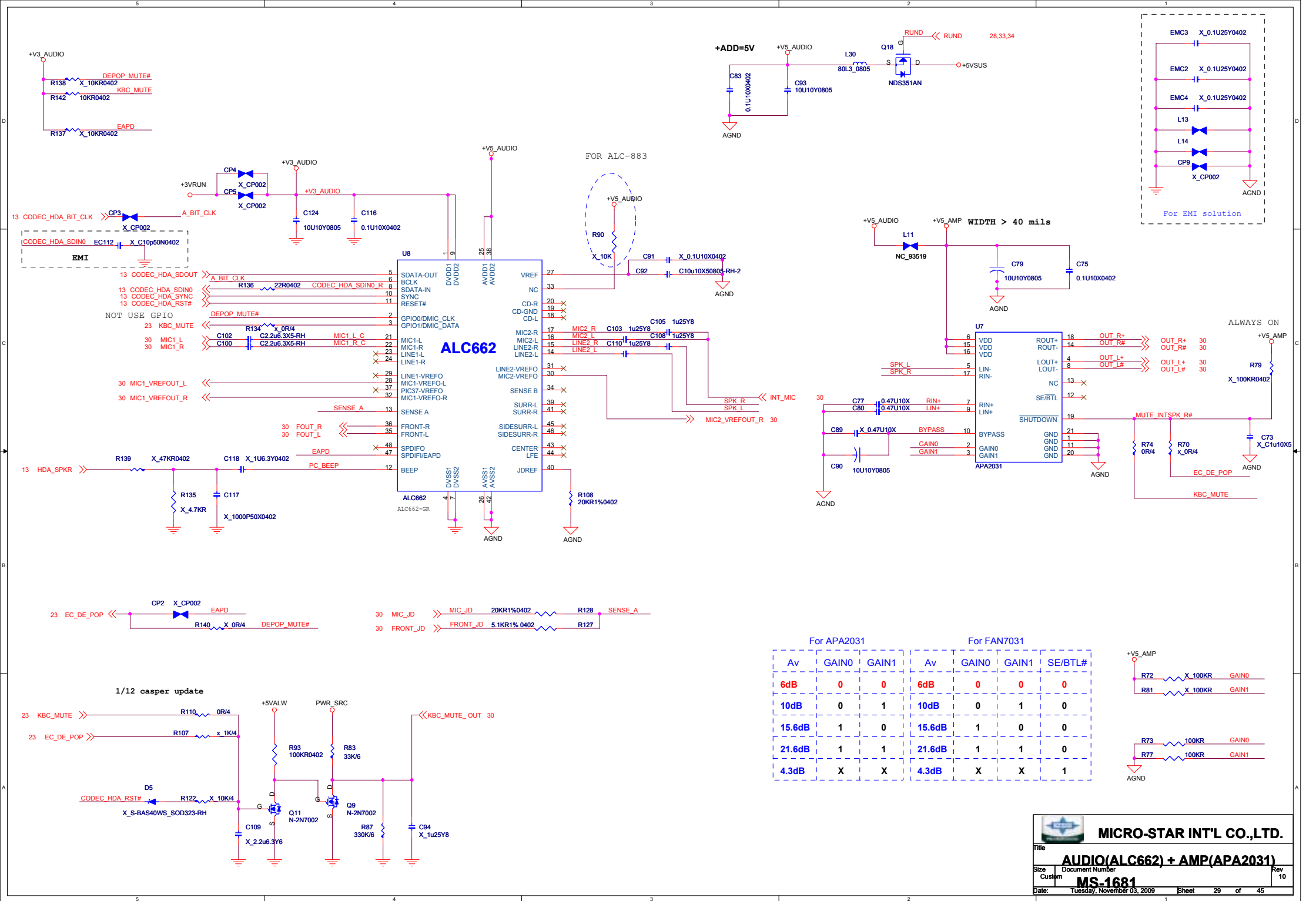
## SATA ODD



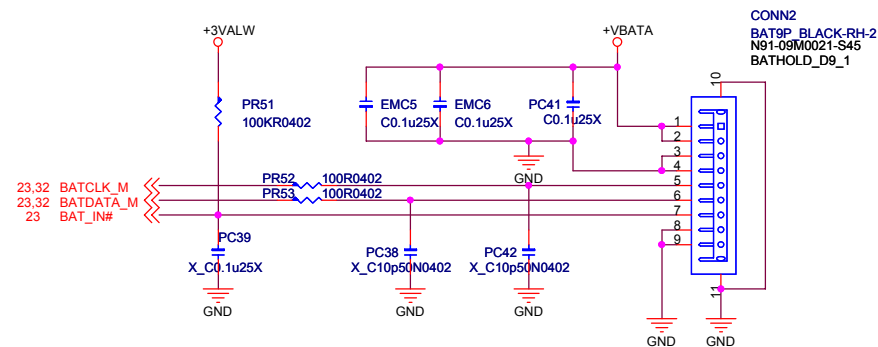
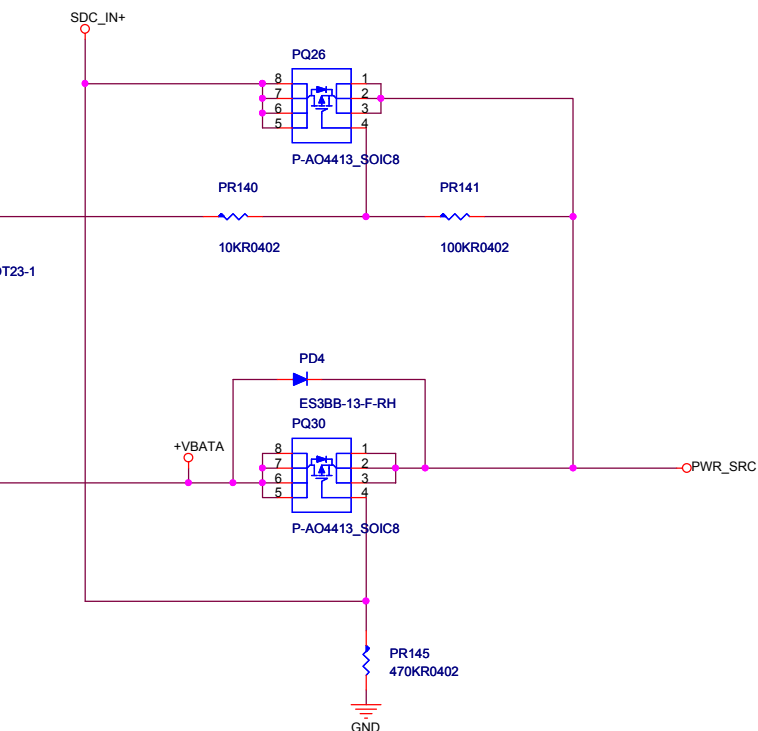
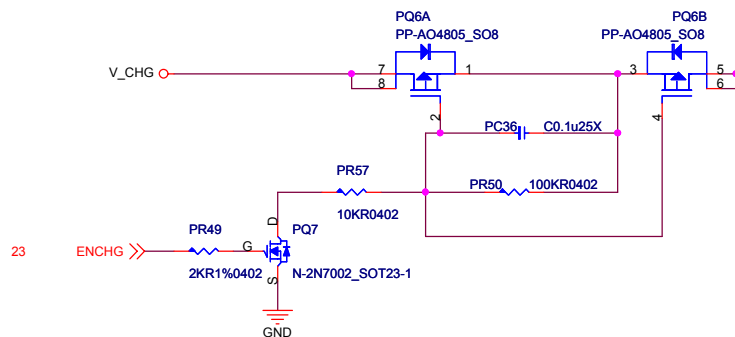
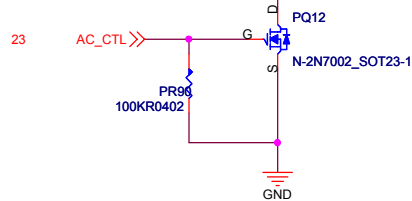
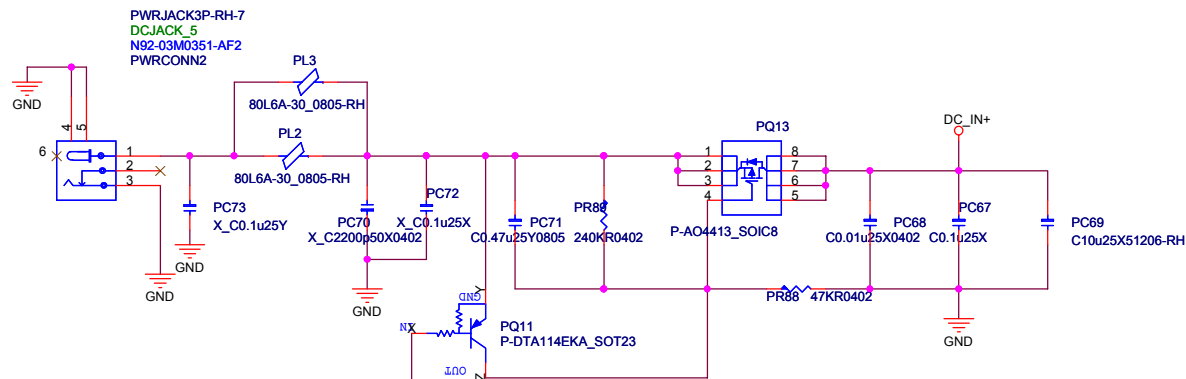
## NEW CARD







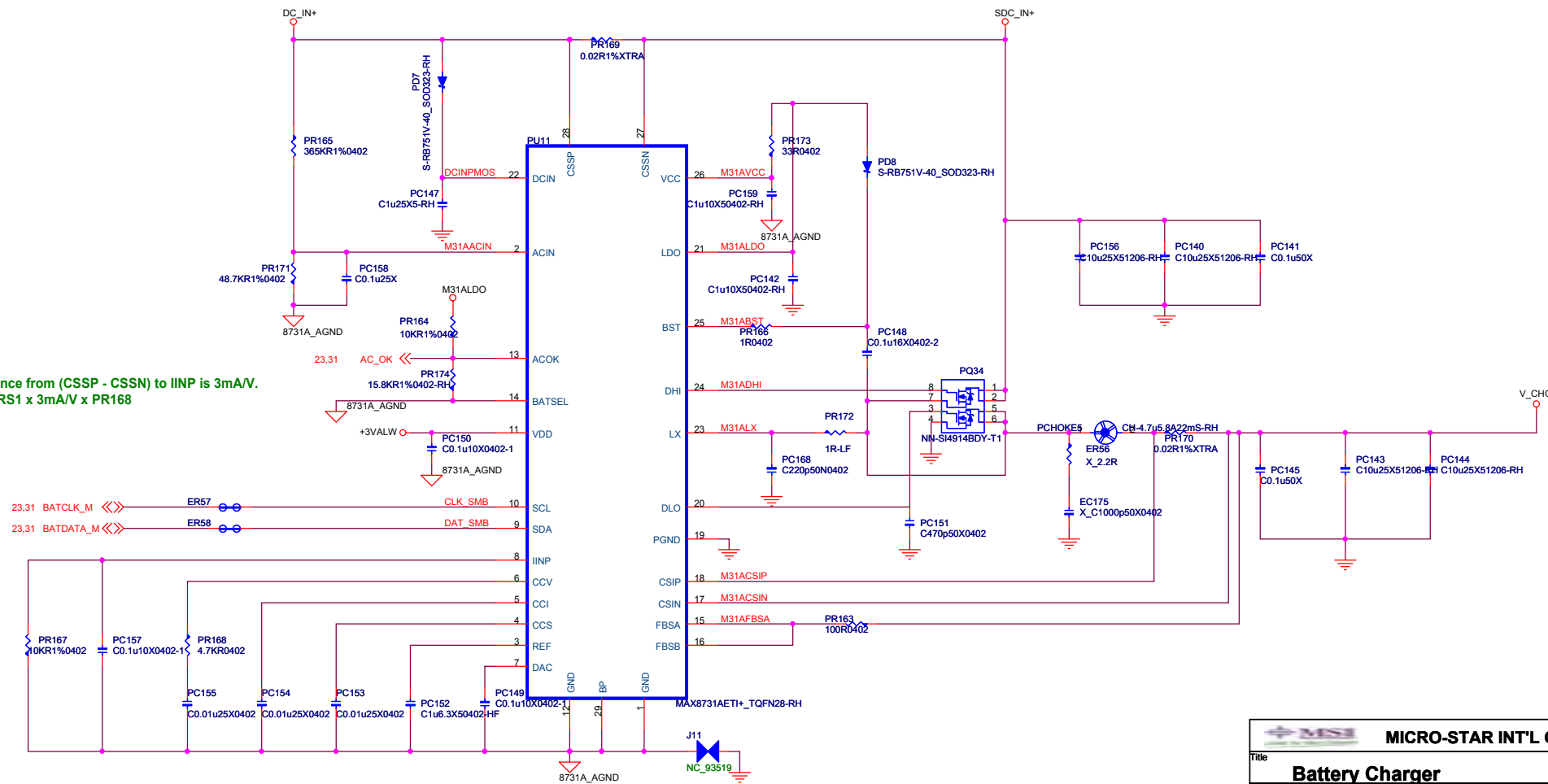




2008/11/14 修改


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```
Adapter= 65W
Adapter input voltage set 19 Voltage
```

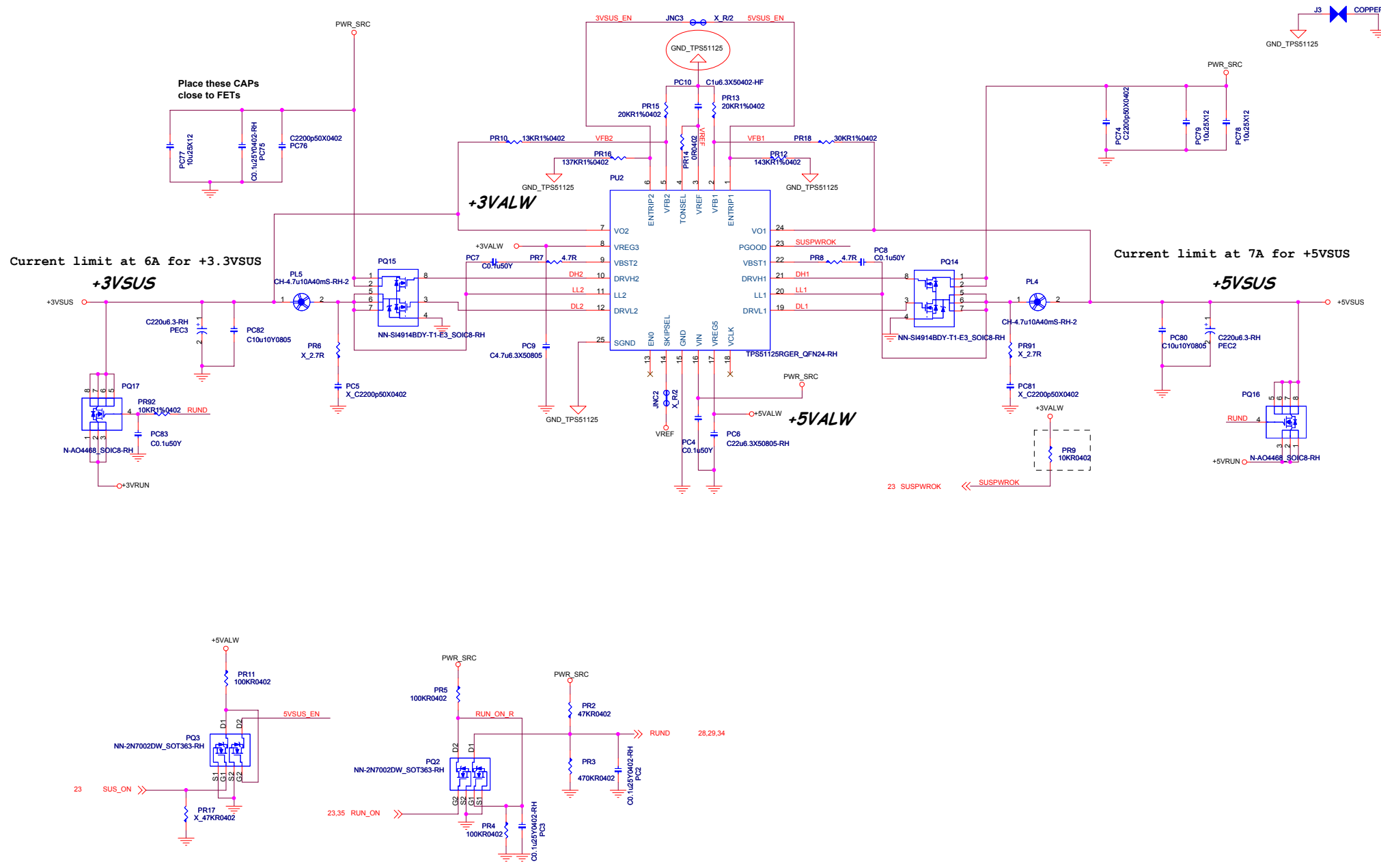


IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2.  $V_{IINP} = IINP_{INPUT} \times RS1 \times 3mA/V \times PR168$

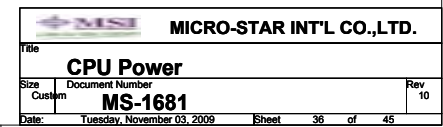
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<b>Battery Charger</b>			
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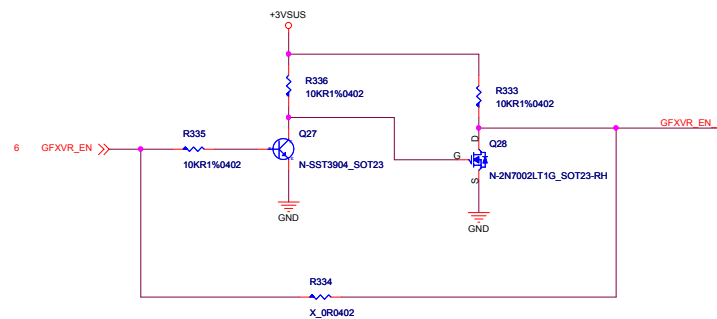
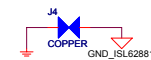


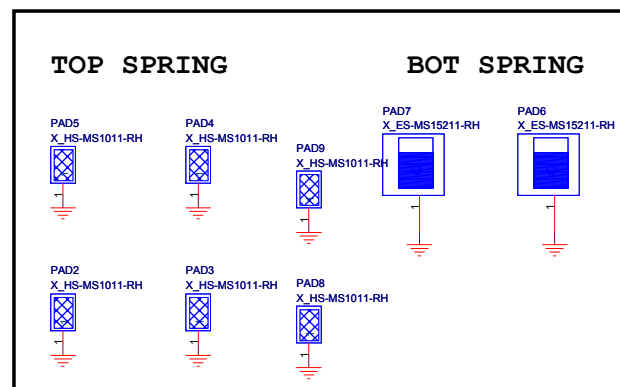
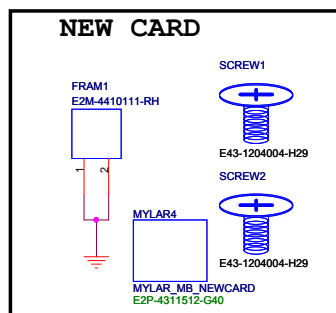




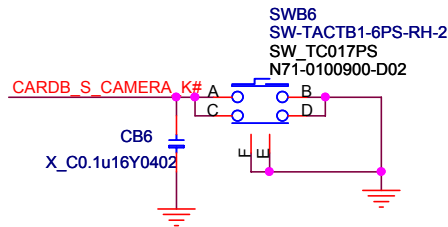
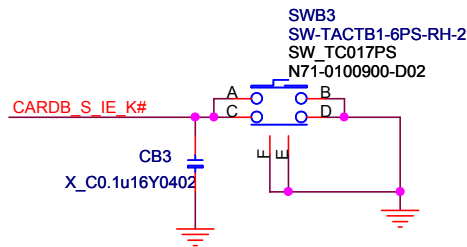






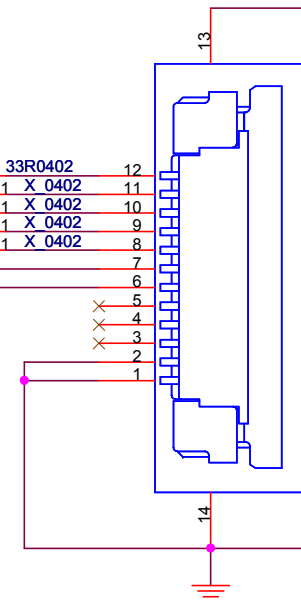




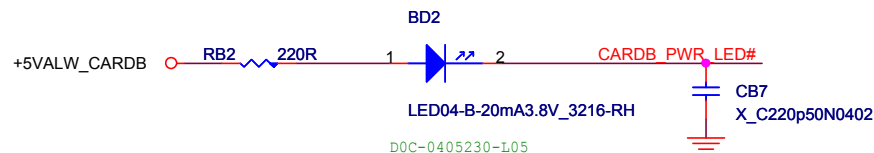
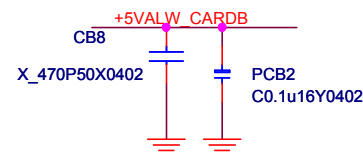
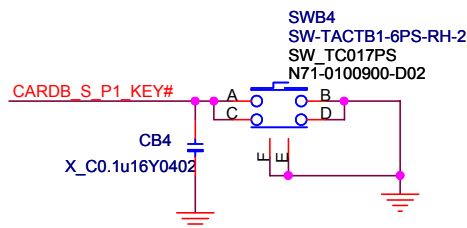
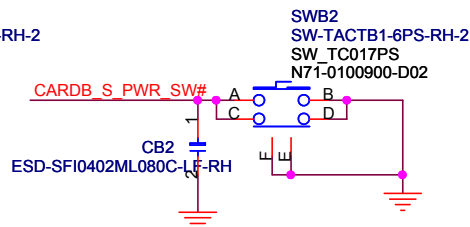
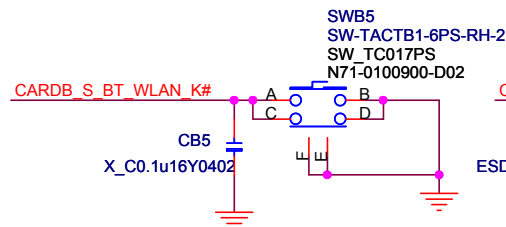


## CARD\_B\_ BOTTOM

CARDB_S PWR SW#	RB3	33R0402	12
CARDB_S BT WLAN K#	JNCB5	2	1 X 0402
CARDB_S CAMERA K#	JNCB6	2	1 X 0402
CARDB_S IE K#	JNCB3	2	1 X 0402
CARDB_S P1 KEY#	JNCB4	2	1 X 0402
CARDP_PWR_LED#			
+5VALW_CARDB			

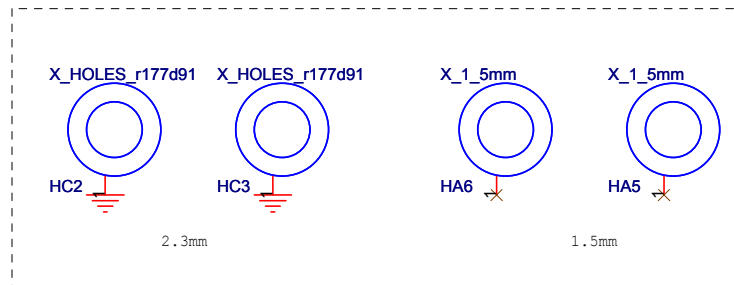


FPC3  
FPC12P-B-0.5PITCH\_WHITE-RH-3  
N5A-12F0200-A81  
FPC\_S12\_3



MYLAR2  
MYLAR\_BOTTOM\_TOP  
E2M-6811111-G40

MYLAR3  
MYLAR\_BACK  
E2P-6811311-G40

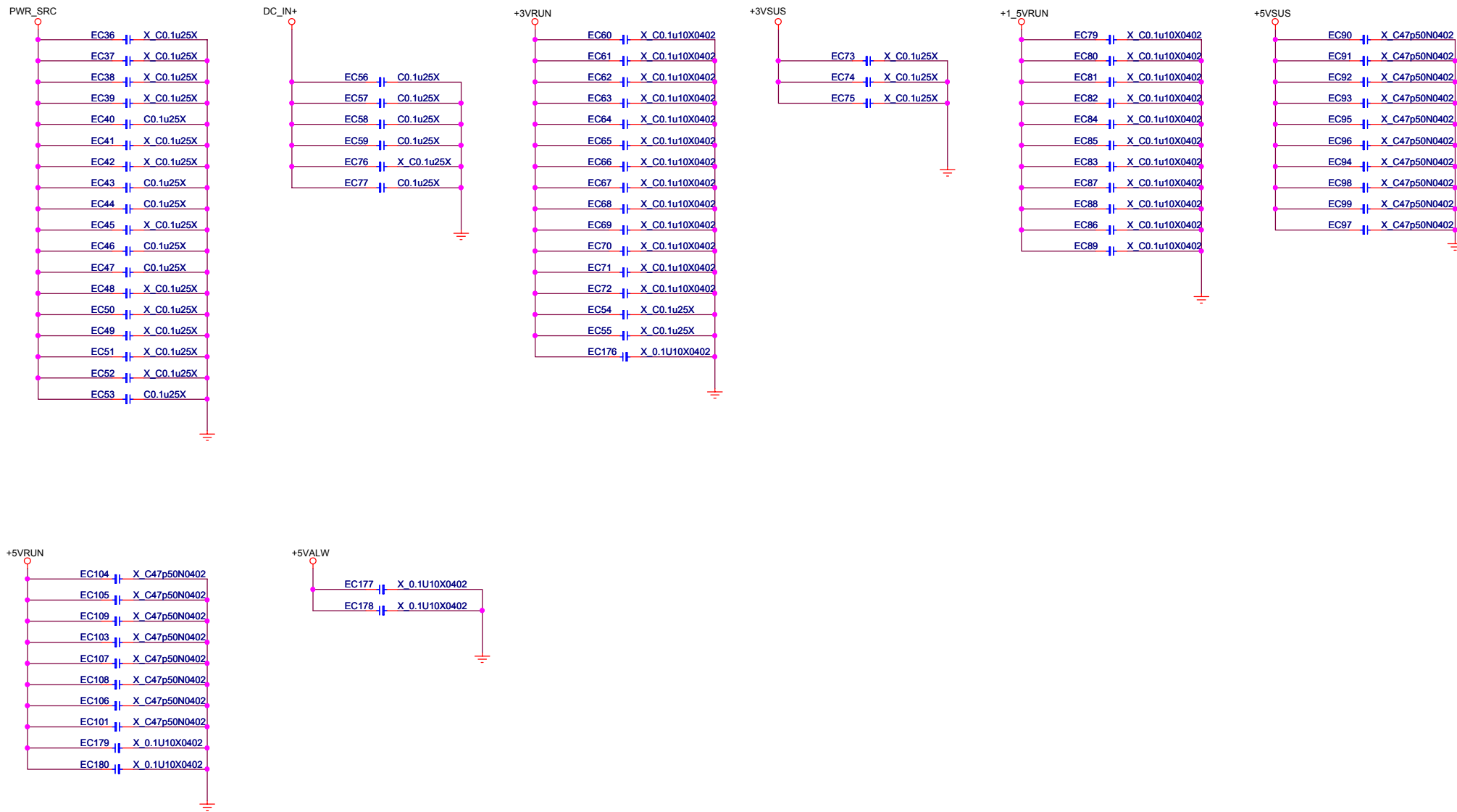


PCBA2  
PCB  
P30-1681B10-D05

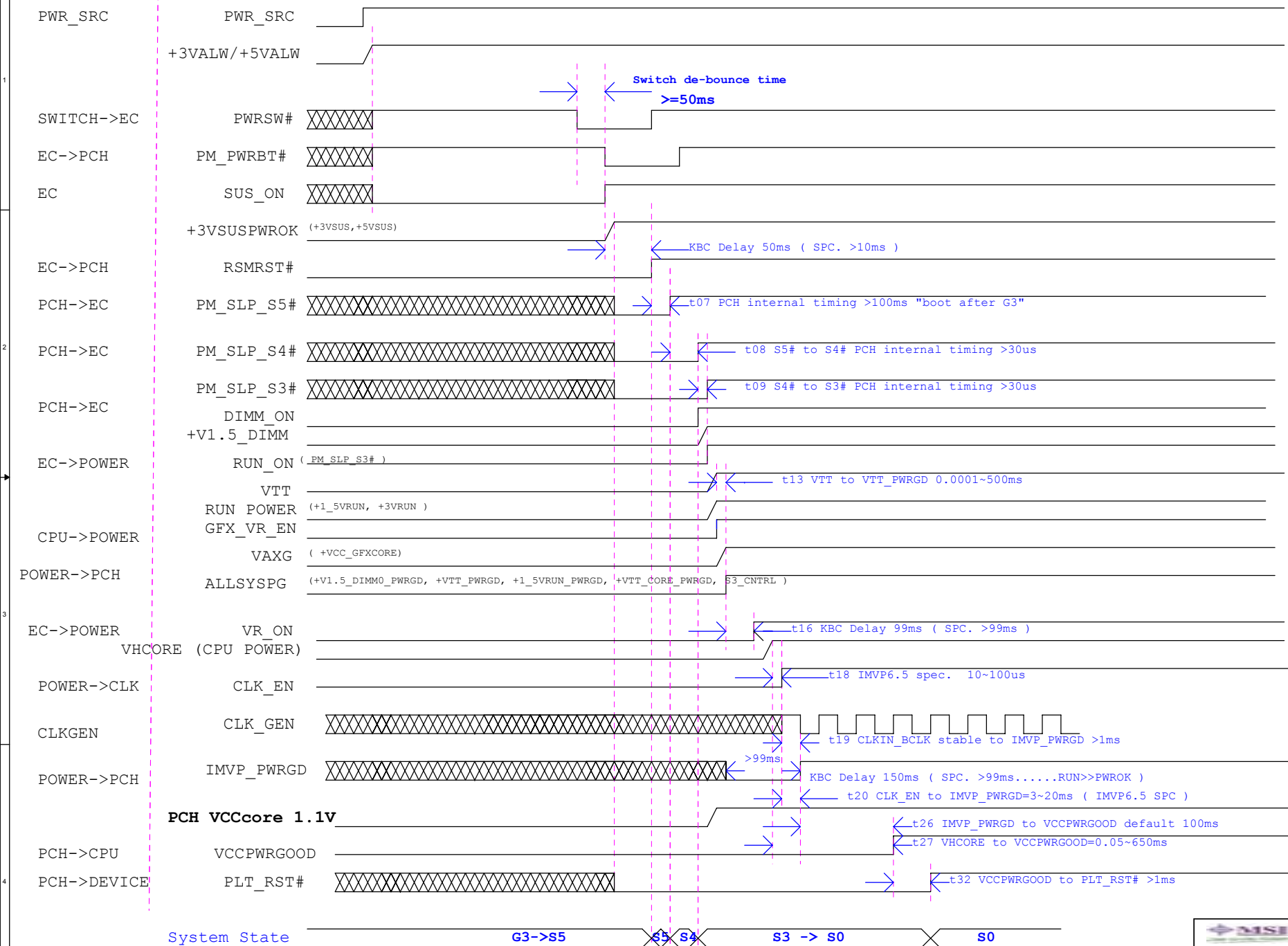
P30-1681B10-H73, 瀚宇博德 (薩摩亞)  
P30-1681B10-D05, 昆穎 (定穎大陸)

			<b>MICRO-STAR INT'L CO.,LTD.</b>		
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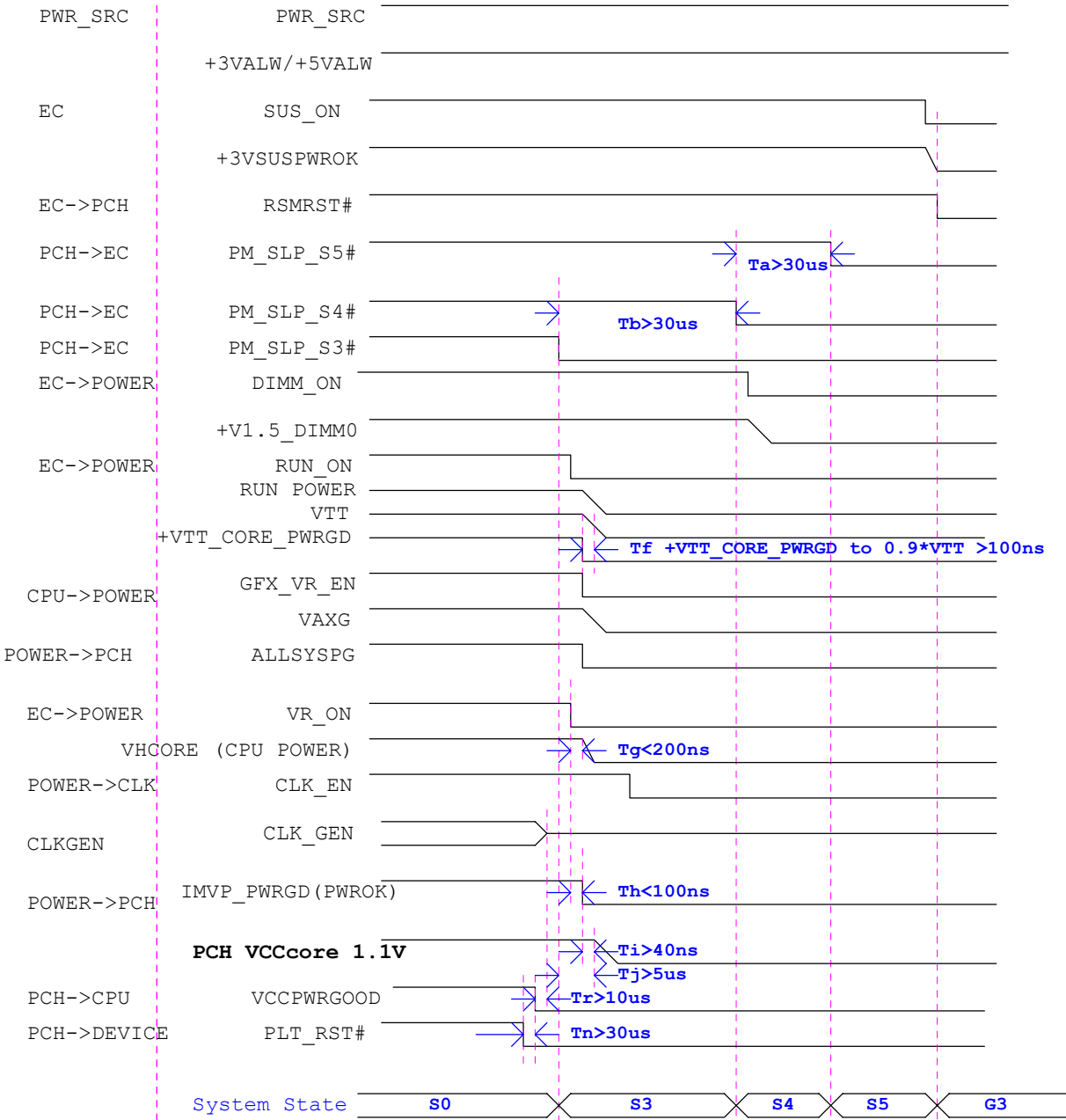


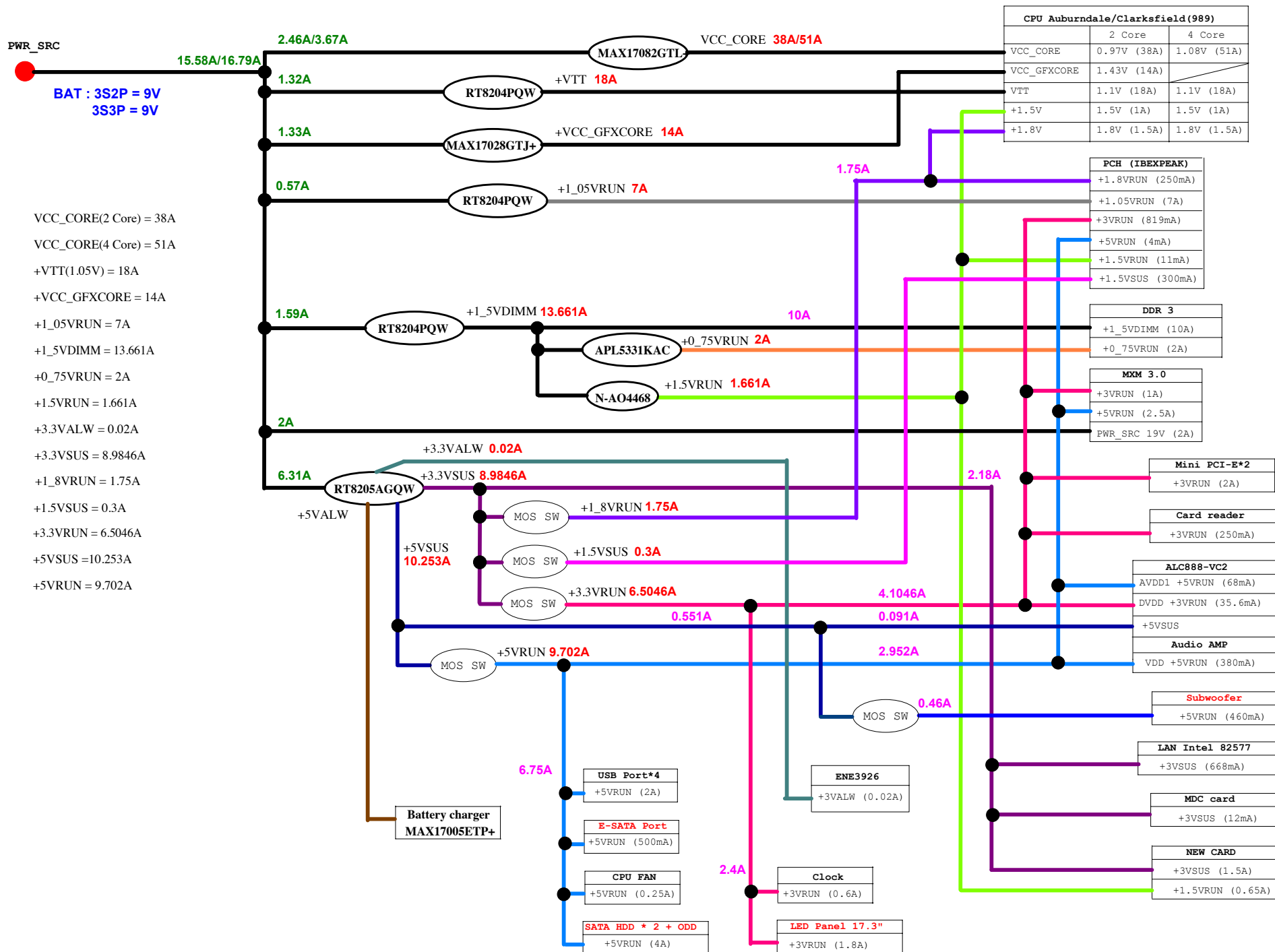


## Calpella System Power on Sequence DC mode



Power down Sequence DC mode S0 to G3





2008/11/13 修改


# Change Note :

## 0A-->0B

- 1.P19 stuff R113 & C85 for intel document about Braidwood
- 2.P23 add one PWM Pin for co-lay LED panel by EC
- 3.P25 Change CardReader to ENE
- 4.P26 Change "LED\_HDD#" PU +5VRUN to +3VRUN
- 5.P26 Fan conn footprint change back to "53398\_03"
- 6.P28 Add Wireless & Bluetooth combo(MS-3870)
- 7.P32 Change PR171 to 48.7K & PR172 to 1R0603
- 8.P33 Change PU2 from "UP6182AQAG" to "TPS51125" & PR18 to 30K
- 9.P34 Change PU9 from "UP6111AQDD" to "UP6128A" & PR156 to 3.48K & PR159 to 10.7K & PQ10 to "D03-0443033-V02"
- 10.P35 Change PU8 from "UP6111AQDD" to "UP6128A" & PR149 to 4.22K & remove C394
- 11.P36 Change PR95 to 1.82K & PR29 to 9.31K & PC90 to 47nf & PR99 to 931R & no stuff PC84 , PR94 , PEC4 , PEC5 , PEC6 , PEC8

## 0B-->10

- 1.P13 add net "TP\_HDA\_DOCK\_EN#\_R" for flash protect control.
- 2.P14 add wimax ac adepter schematic.
- 3.P23 add ENE GPIO13 for flash protect control.
- 4.P25 no stuff C399 & C400 for cardreader detect issus.
- 5.P26 change R307 from 0R to 33R for EMI.
- 6.P31 add 2 cap in +VBATA for EMI.
- 7.P34 change R329 from 0R to 1K for current limit.
- 8.P37 no stuff +VCC\_GFXCOPE PQ23 no cost down.
- 9.P40 change JNCB2 to RB3 , and 33R for EMI.
- 10.P40 change CB2 from 0.1u to 300p for EMI.

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